MAJORITY VOTER CIRCUITS OF TMR CONFIGURATION – A CMOS VLSI DESIGN APPROACH

V. Elamaran, M. Chandrasekar, G. Venkat Babu, Har Narayan Upadhyay

Department of ECE, School of EEE, SASTRA Deemed University, Thanjavur, India

Abstract: Mission, safety and business-critical applications need uninterrupted operation with correct results. But due to the technology shrinking, the microelectronic circuits can be affected by many faults like permanent, transient and intermittent. So, there is a huge demand in designing fault-tolerant systems. Hardware redundancy configurations have been widely used to protect or mask faults. In this research article, to mask multiple faults, N-modular redundancy (NMR) configurations are deployed, namely 3-MR, 5-MR and 7-MR configurations which are implemented to mask one, two and three function module errors respectively. This study primarily focuses on majority voters (MV) of 3-MR configuration. Six MV circuits are proposed and the simulation results are compared with the existing MV circuits. The layouts of each are generated using Microwind tool using 120 nm technology with BSIM4 Spice simulation parameters. Simulation results reveal that the proposed MV circuits obtain better results than the existing methods.

Keywords: ASIC, Majority voting, fault-tolerant, TMR, CMOS VLSI.

1. Introduction

In the recent years, the operational frequencies of digital microelectronic circuits have raised to multi GHz with technology scaling. Integrated circuits are using smaller devices, gates and transistors due to the technology shrinking and the result is the vibrant possibility of occurrences of transient faults or soft errors in a circuit. These soft errors occur mainly due to reduced power supply voltages, cosmic rays, and the deep-submicron (DSM) electromagnetic noises. It is practically difficult to detect or spot such faults. So there is a need to improve the reliability of the digital integrated circuits and systems. This is achieved by deploying in-built fault-tolerant designs in the system [1,2].

The reliability issues are the major concern in all fields of Science and Engineering especially in mission-critical applications like Banking services, Aerospace, Avionics, and Medical Engineering Technologies, etc. The main objective of our study is to protect faults in a system and hence to obtain the fault-free response of the system for the betterment of reliability. The hardware redundancy is the most common technique used to design a fault-tolerant system [3,4].

Triple Modular Redundancy (TMR) is a common approach in digital design, which can be applied for combinational and sequential logic, memory elements, and routing switches, etc. A TMR is the one in which two duplicate copies of the original function module are placed along with the actual module; if one module fails or fault occurs in a module, the error-free output is obtained by computing the majority among all the modules as in Figure 1. This method is the simple but cost-effective due to duplication of modules. Majority voting redundancy is the popular method for fault-tolerant designs in many applications [5,6].
In realizing real time signal and image processing systems, VLSI technology plays a crucial role. For example, in the applications like multimedia, speech processing, medical imaging, mobile wireless applications, space imaging applications, cognitive and software defined radio, data compression and routing, aerial imaging and wearable computers, VLSI technology and signal processing together plays a vital role in implementing those systems [3].

2. Related Work

To protect or mask single module fault, TMR configuration can be used with appropriate majority voter circuit. The existing majority voter (MV) circuits of TMR configuration are described here.

2.1. Conventional Method

In a TMR configuration, let A, B, and C are the outputs of three function modules. The expression of a 2 out of 3 majority voter (conventional method) which is expressed as [7–9],

\[ V = AB + BC + CA \]  \hspace{2cm} (1)

The digital schematic and the truth table of 2 out of 3 majority voter are shown in Figure 2 and Table 1 respectively.

Figure 2. Conventional majority voter of a TMR configuration.
Table 1. Truth table of the majority voter of a TMR configuration

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

2.2. MV circuit using NAND Gates

In the field of CMOS VLSI design, NAND and NOR gates consume less area than AND and OR gates respectively. Figure 3 shows the MV circuit using NAND gates and the voter output is expressed as [7–9],

\[ V = \overline{A\overline{B}} \overline{B \overline{C}} \overline{C A} \] \hspace{1cm} (2)

Figure 3. Majority voter using NAND gates.

2.3. MV circuit using NOR Gates

Figure 4 shows the MV circuit using NOR gates and the voter output is expressed as [7–9],

\[ V = (A + B) + (B + C) + (C + A) \] \hspace{1cm} (3)
2.4. MV circuit using Mux and XOR gate

Figure 5 shows the MV circuit using 2:1 multiplexer & XOR gate and the voter output is expressed as [7–10],

\[ V = (B \oplus C) A + (\overline{B \oplus C}) B \]  

(4)

3. Materials and Methods

The six proposed MV circuits of TMR configuration are described here.

3.1. First Proposed MV circuit

The first proposed MV circuit is imbibed based on carry look-ahead adder (CLA) principle and presented in Code 1; the voter output is expressed as [11],

\[ C_{i+1} = (A_i \oplus B_i)C_i + A_iB_i \]  

(5)

**Code 1.** Pseudo code of the first proposed MV of TMR
If $A \neq B$ then

\[ V = C \]

Else

\[ V = (AB) \]

End

The corresponding schematic is shown in Figure 6.

Figure 6. The first proposed MV circuit of TMR

3.1.1. Results and Discussion (First Proposed MV of TMR)

This circuit requires one 2-input XOR gate, two 2-input AND gates and one 2-input OR gate with a total of 24 transistors (12 nMOS and 12 pMOS). This circuit requires a critical path delay (0.480 ns) as the path follows [11]

Critical path: XOR2 – AND2 – OR2

The larger delay is due to multiple (three) levels. This circuit dissipates more power (6.068 µW) due to the higher switching activity contributed by XOR2 gate.

3.2. The Second Proposed MV of TMR configuration

The second proposed MV circuit is designed with a slight modification in the first proposed MV circuit and the voter output is expressed as [11],

\[ C_{i+1} = (A_i + B_i)C_i + A_iB_i \]  \hspace{1cm} (6)

The corresponding schematic is shown in Figure 7.

Figure 7. The second proposed MV circuit of TMR

3.2.1. Results and Discussion (Second Proposed MV of TMR)
This circuit requires two 2-input OR gates and two 2-input AND gates with a total of 24 transistors (12 nMOS and 12 pMOS). This circuit requires a critical path delay (0.480 ns) as the path follows

Critical path: OR2 – AND2 – OR2

The larger delay is due to multiple (three) levels as similar to the first proposed MV circuit. This circuit occupies more area (128.5 µm²) due to the realization OR gate by inverting the NOR gate. But this circuit dissipates less power (1.232 µW) due to the lower switching activity contributed by OR2 gate than XOR2 gate in the first proposed MV circuit.

3.3. The Third Proposed MV of TMR configuration

The third proposed MV circuit is imbibed and presented in Code 2. The corresponding schematic is shown in Figure 8.

**Code 2.** Pseudo code of the third proposed MV of TMR

```plaintext
If (A=0) then
    V = (BC)
Else
    V = (B+C)
End
```

![Figure 8. The third proposed MV circuit of TMR](image)

3.3.1. Results and Discussion (Third Proposed MV of TMR)

This circuit requires one 2-input OR gate, one 2-input AND gate and one 2:1 multiplexer with a total of 18 transistors (9 nMOS and 9 pMOS). This circuit requires a critical path delay (0.260 ns) as the path follows

Critical path: AND2 – MUX2

Since the AND and OR gates are implemented with NAND followed by an inverter and NOR followed by an inverter respectively, higher switching activities are involved. And hence this circuit dissipates larger power (3.959 µW) and OCCUPIES more area (99.8 µm²).
3.4. The Fourth Proposed MV of TMR Configuration

The fourth proposed MV circuit is imbibed and presented in Code 3. The fourth proposed MV circuit is designed using three 2:1 Multiplexers as illustrated in Figure 9.

**Code 3.** Pseudo code of the fourth proposed MV of TMR

```plaintext
If (A=B) then
    If A=0 then
        V = 0
    Else
        V = 1
    Else
        V = C
End
```

![Figure 9. The fourth proposed MV of TMR](image)

3.4.1. Results and Discussion (Fourth Proposed MV of TMR)

This circuit requires three 2:1 multiplexers and hence occupies more area (168.2 µm²) with a total of 18 transistors (9 nMOS and 9 pMOS). This circuit requires a lower critical path delay (0.2 ns – due to only two levels) as the path follows

Critical path: MUX2 – MUX2

3.5. The Fifth Proposed MV of TMR Configuration

The fifth proposed MV circuit is designed based on the expression as [11]

\[ V = \overline{AB}(A + B)C + AB \] (7)

The corresponding schematic is illustrated in Figure 10.
3.5.1. Results and Discussion (Fifth Proposed MV of TMR)

This circuit requires one 2-input NAND gate, two 2-input OR gates, one inverter and one 3-input OR gate with a total of 26 transistors (13 nMOS and 13 pMOS) and hence with a higher critical path delay (0.55 ns) as the path follows

Critical path: NAND2 – AND3 – OR2

This circuit occupies considerably small area (83 µm²) due to the AND realization by the inverting the NAND2 and shared appropriately.

3.6. The Sixth Proposed MV of TMR Configuration

The sixth proposed MV circuit is imbibed and presented in Code 4. The corresponding schematic is shown in Figure 11.

**Code 4. Pseudo code of the sixth proposed MV of TMR**

```plaintext
If (\( A \oplus B = 1 \)) then
  \( V = C \)
Else
  If (\( \overline{AB} = 1 \)) then
    \( V = 0 \)
  Else
    \( V = 1 \)
End
```
3.6.1. Results and Discussion (Sixth Proposed MV of TMR)

This circuit requires one 2-input NAND gate, two 2:1 multiplexers and one 2-input XOR gate with a total of 22 transistors (11 nMOS and 11 pMOS) and hence with larger area (158.3 µm²) with higher power dissipation (7.656 µW). This circuit obtains a lower critical path delay (0.360 ns) due to 2:1 multiplexer contributions as the path follows

Critical path: NAND2 – MUX2 – MUX2

4. Simulation Results with MV circuits of TMR

The critical path delay, area and power are the performance metrics used for the comparison among the existing and proposed majority voter circuits. The figure-of-merit (FOM) metric is calculated as the reciprocal of the product of power, delay, and area to identify an optimal configuration. Minimization of power, delay and area is desirable. Hence for the optimized design, a higher FOM value can be considered.

The simulation results of the existing and proposed MV circuits of TMR configuration are summarized here. Figure 12 shows that the electrical simulation results of a MV of TMR configuration. The simulation results of the existing and proposed MV circuits of TMR configuration are presented in Table 2. Simulation results are obtained using Microwind and DSCH computer aided automation tools [12,13]. Simulation results reveal that the proposed MV circuits obtain better results than the existing MV circuits.
Figure 12. Electrical simulation (SPICE) results of a MV of TMR configuration with $V_{DD} = 1.2$ V and $V_{SS} = 0$V

Table 2. ASIC Implementation Results

<table>
<thead>
<tr>
<th>Voter Design</th>
<th>Platform</th>
<th>Delay (ns)</th>
<th>Area cell ($\mu$m$^2$)</th>
<th>Power ($\mu$W)</th>
<th>FOM $\times 10^3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>ASIC 120 nm</td>
<td>0.29</td>
<td>83.0</td>
<td>4.865</td>
<td>8.53</td>
</tr>
<tr>
<td>NAND gates</td>
<td>ASIC 120 nm</td>
<td>0.32</td>
<td>99.7</td>
<td>1.249</td>
<td>25.00</td>
</tr>
<tr>
<td>NOR gates</td>
<td>ASIC 120 nm</td>
<td>0.29</td>
<td>54.5</td>
<td>2.810</td>
<td>22.50</td>
</tr>
<tr>
<td>2:1 Mux &amp; XOR</td>
<td>ASIC 120 nm</td>
<td>0.26</td>
<td>79.5</td>
<td>3.712</td>
<td>13.03</td>
</tr>
<tr>
<td>Proposed 1</td>
<td>ASIC 120 nm</td>
<td>0.48</td>
<td>72.3</td>
<td>6.068</td>
<td>4.74</td>
</tr>
<tr>
<td>Proposed 2</td>
<td>ASIC 120 nm</td>
<td>0.48</td>
<td>128.5</td>
<td>1.232</td>
<td>13.15</td>
</tr>
<tr>
<td>Proposed 3</td>
<td>ASIC 120 nm</td>
<td>0.26</td>
<td>99.8</td>
<td>3.959</td>
<td>9.73</td>
</tr>
<tr>
<td>Proposed 4</td>
<td>ASIC 120 nm</td>
<td>$0.2$</td>
<td>168.2</td>
<td>3.730</td>
<td>7.90</td>
</tr>
<tr>
<td>Proposed 5</td>
<td>ASIC 120 nm</td>
<td>0.55</td>
<td>83.0</td>
<td>5.649</td>
<td>4.35</td>
</tr>
<tr>
<td>Proposed 6</td>
<td>ASIC 120 nm</td>
<td>0.36</td>
<td>158.3</td>
<td>7.656</td>
<td>2.29</td>
</tr>
</tbody>
</table>

5. Conclusion

The six proposed MV circuits of TMR configuration were studied & analyzed and also the simulation results were compared with the existing circuits. Simulation results reveal that the fourth proposed MV circuit obtains lower delay than others and also the second proposed MV circuit dissipates lower than others. The first proposed MV circuit occupies less area (second
best) than others; the fifth proposed MV circuit rank in third. The second proposed MV circuit obtains better (third best) FOM result than others.

References