A Low Power Fault Tolerant Architecture for Digital Systems

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Abstract: The paper unveils a design strategy to counteract the presence of faults in digital systems and uphold their reliability. The proposed work endeavours to develop an augmented version of Triple Modular Redundancy (TMR) to neutralise the effect of faults present in digital systems. The work focuses on developing a reconfigurable TMR based fault tolerant architecture to stand against the incursion of both hard and soft errors. The scheme intends to reduce the power consumption of fault tolerant methodologies with the view to maintain the area overhead remains almost on par with other strategies in use. The built-in fault tolerant ability of the design ensures digital systems to provide true outputs even in the presence of faults. The Modelsim based simulation results obtained for the digital circuit chosen for analysis ascertains the fault tolerant ability of the proposed methodology and the use of Xilinx 9.2i foundation series with an FPGA as the target device ensure its practical feasibility. The results proclaim the sheer merits of the scheme in terms of reduction in power consumption by a factor of 33% than the traditional TMR architecture.

Keywords: Fault Tolerance, Power Consumption, Reliability, TMR.

1. Introduction

The sensational development in the field of semiconductor technology has made the transition of digital systems possible from application specific to almost all areas that include earth applications to space research. This remarkable journey of semiconductor technology rides on the evolution of Complementary Metal Oxide Semiconductor (CMOS) technology which enables the mass production of smaller and cheaper Integrated Circuits (IC) with higher performance and lower power consumption [1].

However, the very technological advancements hold the key responsibility for the error prone nature of digital systems in the sense the reduction in feature size as well as supply voltage adversely influence their reliability [2]. The appearance of faults during the design or manufacturing or operational phase remains the root cause of malfunction of digital devices which in turn ultimately leads to system failure. The faults that may be temporary or permanent in nature degrade the performance of the system and reduce its life time [3]. Thus, the fault tolerant phenomenon gains crucial significance as it ensures reliable performance and extends the life time of the system.

A wide variety of factors manifest themselves as the root cause for the occurrence of temporary and permanent faults in digital systems. The fabrication process of smaller devices becomes extremely difficult and leads to manufacturing defects that remain as the primary source of hard errors. Even digital systems with fault free design may suffer from supply voltage fluctuations, temperature variations and interference issues during the operational phase. The vulnerability of smaller transistors towards radiation effects leads to soft errors in the form of Single Event Transients (SETs) in combinational logic and may end up as Single Event Upset (SEUs) in sequential elements [4,5]. Further, quite naturally the ageing phenomenon remains the cause for the occurrence of intermittent faults which possess the potential to turn out to be permanent faults when left untreated and end up as hard errors during the twilight period of digital systems.
The design process of present day digital systems remains a challenge due to the continual introduction of fresh and new CMOS technological nodes and therefore the traditional way of treating faults at the physical level and bringing changes in manufacturing process appears to be no longer feasible [6]. It augurs the need of fault tolerant techniques being inherently able to tackle faults even at the design level and enable to meet the reliability requirements of modern day digital circuits and systems.

The fault tolerant schemes should possess the ability to protect the system against the faults of different nature that may either be temporary or permanent. The design of fault tolerant digital systems critically orients towards power consumption especially in advanced CMOS technology besides the eternal quest for low area overhead. Thus, the design of low power consuming fault tolerant schemes without compromising area overhead requirements remains the most sought after in industry [7].

Having thoroughly considered the pressing demands of present day digital system design, the work engages itself to develop a design strategy to tolerate the ill effects of both temporary as well as permanent faults occurring in digital circuits and systems. The proposed architecture houses three identical modules of the circuit under test much similar to the best known TMR approach in which three logic circuits run in parallel [8,9]. On the contrary, the scheme contrasts itself from the traditional TMR architecture as it mandates only two modules among the three to operate at any given point of time which results in the reduction of dynamic power by a factor of 33% and the exiguous increase in area overhead.

The rest of the paper organizes itself under four headings that include literature review, design methodology, results and discussion and finally conclusion.

2. Literature Review

A fault tolerant design for combinational logic and sequential elements has been proposed in [10] which combines parity check codes and duplication strategy in an effort to provide diagnosis and correction capabilities to the design besides error detection abilities. An analysis on how two key trends in microprocessor technology – device scaling and super pipelining –have an impact on the soft error rate in CMOS memory and logic circuits has been presented in [11].

A variety of Built-in Self-Repair (BISR) approaches for memories affected by high defect densities has been proposed in [12]. A Built-In Soft-Error Resilience (BISR) technique for radiation induced soft errors in latches and flip flops has been presented in [13].

An error tolerant Dynamic Voltage Scaling (DVS) technology with in-situ timing error detection and correction capabilities called RAZOR has been proposed in [14]. Further, a RAZOR flip-flop with the ability to double sample the pipeline stage values has been introduced. A new design methodology named as RAZOR II implementing a flip-flop with in-situ error detection and correction capabilities for variation induced delay errors has been presented in [15].

The sensitivity of SETs towards CMOS scaling has been addressed and the behaviour of SETs from particle physics to circuit level examined besides the conduct of soft error analysis in digital circuits in [16]. A soft error correction scheme for embedded storage elements in level sensitive designs has been presented with a view to detect and locate SEUs in [17].

The conditions that make the use of TMR architecture interesting for the exclusive purpose of yield improvement has been analysed in [18]. The test requirements for the TMR architecture have been examined and a solution proposed for the generation test patterns for such architectures.

In-spite of the continual efforts being made towards fault tolerance of modern day digital systems, there exists a need to come up solutions providing power saving besides fulfilling area overhead demands.

3. Design Methodology

The proposed scheme intends to protect the target system from various forms of faults that occur during normal operation of digital systems and reiterate its promise to enable the system to provide reliable performance even in the presence of faults. It focuses on the reliability issues of combinational logic of digital circuits which in turn ensures authenticity in the performance of digital systems on a larger periphery.

Similar to TMR, the architecture houses three identical logic circuits besides a comparator, a switching unit and a control unit. It formulates a reconfigurable TMR architecture in the sense the two out of the three identical logic modules involves themselves in operation and the other remains
standby in any one of the three configurations in action at any given point of time. In other words, it employs three different configurations in its fault tolerant pursuit and only one configuration remains in operation making two of the three identical logic circuits run in parallel at any given point of time leaving the other being standby. The switching unit holds the responsibility for the selection of a particular configuration in accordance with the directive from the control unit which actuates the control signal to make or break the configuration subject to the outcome of the comparator.

The comparator authenticates the proper functioning of the configuration in use and ensures the fault free operation with a logic 0 output when no faults present in the system. On the contrary, it produces a logic 1 output when it senses the presence of faults in any of the two modules run in parallel for the current configuration. The active high output of the comparator mandates the control unit to break the present configuration and make the next configuration in line with a view to tolerate the faults in the system.

The scheme reaps the benefit of combining both information redundancy and hardware redundancy together in the process of detecting and tolerating both temporary and permanent faults. The information redundancy aids in the process of detecting the faults while hardware redundancy helps to achieve fault tolerance. The duplication and comparison strategy serves the exclusive purpose of detecting the faults in any of the two logic circuits in operation. The inclusion of the third logic circuit accomplishes the task of tolerating the presence of faults.

The Fig. 1 shows the functional block diagram of the proposed fault tolerant architecture while Fig. 2 illustrates the three different configurations of the fault tolerant design. The design strategy inculcate the system to operate with the first two logic circuits (lc1 & lc2) run in parallel and keep the third logic circuit (lc3) standby in configuration 1 (cnfg 1) in its fault free state. The incursion of faults in either lc1 or lc2 forces the system to switch over to the second configuration (cnfg 2) in which the second and third logic circuits (lc2 & lc3) run concurrently whereas lc1 remains standby. The third configuration (cnfg 3) with lc1 and lc3 run simultaneously and lc2 stays standby comes into effect when the system malfunctions with cnfg2. Thus, only two out of the three logic circuits run at any given point of time and the other remains standby which in turn results in dynamic power saving by a factor of 33%.

4. Results and Discussion

![Figure 1 Fault tolerant architecture](image)

![Figure 2 The three different configurations of the architecture](image)
The Modelsim based simulation results presented from Figs. 3 through 5 relate the sequence of events that occur during the fault tolerant pursuit of the proposed scheme. The result in Fig. 3 illustrates the fault free operating state of the 2:4 decoder designated as the circuit under test whereas the results available in Figs. 4 and 5 elucidate the ability of the proposed strategy to retain the decoder in its fault tolerant state.

The response seen in Fig. 3 explains the fact that the “00” output of the control unit (cont) implies the fault free operation of the circuit and keeps cnfg1 in action in which lc1 and lc2 run in parallel while lc3 remains standby. It is seen that the two functioning modules lc1 and lc2 provide the output as “1000” and the primary output signal (dout) reflects the same for a given input combination of “11” and at the same time the output of lc3 is in high impedance state as it remains as standby in cnfg1.

![Fig. 3 Response of the circuit with cnfg1 is in action](image-url)
The appearance of a permanent stuck-at-1 fault on the third output line of lc2 at the 500th ns forces the control unit to change the configuration from cnfg1 to cnfg2 by generating the control signal as “01” which corresponds to the second configuration cnfg2.

The control signal of “01” at the 600th ns enables cnfg2 at the 700th ns which in turn facilitates the concurrent functioning of lc2 and lc3 and keeps lc1 as standby as illustrated in Fig.4.

Fig. 4 Response of the circuit with cnfg2 is in operation
The Fig. 5 narrates the sequence of events which begins with the transition of the control signal from “01” to “10” at the 900th ns which mandates the system to switch over from cnfg2 to cnfg3 at the 1000th ns as the problem lies with lc2. The third configuration cnfg3 employs lc1 and lc3 as the work horses and keep the error prone lc2 aside from action in an effort to provide the true outputs on the primary output lines.
The results obtained for the 2:4 decoder evince the fact that the circuit remains fault tolerant and continues to render its true services even in the presence of faults thanks to the innate ability of the corrective mechanism inherently associated with it. The ability of the design to lay down corrective measures to protect the system against faults and provide reliable performance epitomizes its fault tolerant attribute. Further, the proposed fault tolerant architecture reiterates its promise to tolerate the presence of faults with a dynamic power saving of 33% compared to traditional TMR approach as it employs only two logic circuits out of the three at any given point of time.

Modern day FPGAs receive wide spread use in many fields owing to their ability to reconfigure themselves that too on the run which in makes them much suitable for fault tolerant designs. The real time implementation of the proposed fault tolerant architecture using Xilinx 9.2i foundation series with XC3S500E FPGA serves to validate the simulated performance.

5. Conclusion
A hybrid fault tolerant architecture has been evolved with a view to tolerate temporary as well as permanent faults occurring in digital systems. The procedure has been formulated to sense the occurrence of faults at the combinational logic of digital systems and nullify their negative impact on the system in an effort to bring out the reliable performance. The Modelsim based simulation results obtained for a 2:4 decoder demonstrate the ability of the fault tolerant strategy to enable the circuit to produce true outputs even in the presence of faults. The exclusive benefits of the proposed architecture have been primarily realized in terms of dynamic power saving compared to traditional TMR based fault tolerant systems. The VHDL code developed for the proposed fault tolerant architecture has been experimentally validated with the help of XC3S500E FPGA on Xilinx Foundation series ISE 9.2i.

References


