

RECENT ADVANCES ON AC PV NINE-LEVEL CASCADE INVERTER

¹R.Sathish Kumar, ²D.Srivishnu, ³M.Surendran, ⁴K.Vignesh
^{1,2,3,4}Electrical and Electronics Engineering,
Sri Krishna College Of Technology

Abstract: Asymmetric Cascaded structure electrical converter (ACMLI) was wide studied. Numerous management methods are investigated but, most of the rumored management methods not mentioned a way to determinate voltage levels, firing angle, switching-state and different parameters management style. It focuses on asymmetrical topologies wherever the cell input voltages area unit of various values. These hybrid topologies could be attention-grabbing for many applications. One amongst the most edges is that the high resolution that may be obtained with a tiny low variety of cells. Another profit is that the higher energetic potency of the electrical converter alone. All the same, the requirement of DC-DC converters to produce the cells of reversible structure converters will increase the price and losses of such inverters. It limits their application field. This paper is enforced employing a PIC Microcontroller in order that higher resolution is achieved within the management of structure electrical converter output voltage magnitude and it's verified by experimentation

Keywords: PVcell, MATLAB, hybrid cascaded h-bridge multilevel inverter, carrier-signal PWM, THD.

1. Introduction

An electrical converter takes DC power and converts it in to AC power for running equipment and appliances. Various industrial applications have begun to need higher power equipment in recent years. Some medium voltage motor drives and utility applications need medium voltage and power unit power level. For a medium voltage grid, it's difficult to attach only 1 power semiconductor switch directly. As a result, a construction power device structure has been introduced as another in high power and medium voltage things.

A construction device not solely achieves high power ratings, however additionally permits the utilization of renewable energy sources. Renewable energy sources like electrical phenomenon, wind, and fuel cells will be simply interfaced to a construction device system for a high power application. The idea of a construction device to attain higher power is to use a series of power semiconductor switches with many lower voltage dc sources to perform the ability

conversion by synthesizing a stairway voltage wave shape. Capacitors, batteries, and renewable energy voltage sources will be used because the multiple dc voltage sources. A construction device has many benefits over a standard two-level device that uses high shift frequency pulse width modulation (PWM). The engaging options of a construction device will be shortly summarized as follows. Within the recent years digital management techniques are getting the foremost widespread resolution in trendy power physics applications. The microprocessors, DSP processor and application specific integrated circuits (ASIC) area unit accountable for higher performance of the ability converters nonetheless the look of digitally controlled power physics is stricken by many issues, like rate, package movability, re-usability, peripheral devices and register settings specific for every silicon chip. These issues will be mitigated by PIC microcontroller. Within the following chapters we have a tendency to area unit aiming to discuss regarding the literature survey done why we have a tendency to area unit going for style of construction electrical converter and their implementation in package simulation exploitation Simulink model in Mat work package. Then constant is enforced in hardware exploitation PIC microcontroller and also the check results area unit obtained.

2. Existing System

2.1 Diode clamped inverter

The most usually used structure topology is that the diode clamped electrical converter, during which the diode is employed because the clamping device to clamp the dc bus voltage therefore on deliver the goods steps within the output voltage. A three-level diode clamped electrical converter consists of 2 pairs of switches and 2 diodes. Every switch pairs works in complimentary mode and therefore the diodes used to offer access to mid-point voltage. In a three-level electrical converter every of the 3 phases of the inverter shares a typical dc bus, that has been subdivided by 2 capacitors into 3 levels. The DC bus voltage is split into 3 voltage levels by using 2 series connections of DC capacitors, C1 and C2. The voltage stress across every shift device is limited to V_{dc} through the clamping diodes Dc1 and Dc2. It's assumed that the full dc link

voltage is V_{dc} and middle purpose is regulated at $1/2$ the dc link voltage, the voltage across every electrical condenser is $V_{dc}/2$ ($V_{c1}=V_{c2}=V_{dc}/2$). In a very 3 level diode clamped inverter, there square measure 3 completely different potential shift states that apply the step case voltage on output voltage regarding DC link electrical condenser voltage rate. For a three-level electrical converter, a collection of 2 switches is on at any given time and in a very five-level electrical converter, a set off our switches is on at any given time then on.

2.2 Flying capacitor

A FCMI uses a ladder structure of dc facet electrical condensers wherever the voltage on every electrical condenser differs from that of ensuing capacitor. To generate m-level way output voltage, m-1 capacitors within the dc bus area unit required. Every phase-leg has the same structure. The scale of the voltage increment between 2 capacitors determines the scale of the voltage levels within the output wave shape.

2.3 9 level MLI

The convertor topology is predicated on the series association of single-phase inverters with separate dc sources. The ability circuit for one section leg of a three-level, five-level and seven-level cascaded electrical converter. The ensuing section voltage is synthesized by the addition of the voltages generated by the various cells. During a 3-level cascaded electrical converter every single-phase full-bridge electrical converter generates 3 voltages at the output: $+V_{dc}$, 0, $-V_{dc}$ (zero, positive dc voltage, and negative dc voltage). This can be created attainable by connecting the capacitors consecutive to the ac facet via the ability switches. The ensuing output ac voltage swings from $-V_{dc}$ to $+V_{dc}$ with 3 levels, $-2V_{dc}$ to $+2V_{dc}$ with five-level and $-3V_{dc}$ to $+3V_{dc}$ with seven-level electrical converter. The stairs wave is almost curved, even while not filtering.

2.4 Features of 9level MLI

For real power conversions, (ac to dc and dc to ac), the cascaded-inverter desires separate dc sources. The structure of separate dc sources is well matched for numerous renewable energy sources like cell, electrical phenomenon, and biomass, etc. Connecting separated dc sources between 2 converters during a succeeding fashion isn't attainable as a result of a brief circuit are introduced once 2 succeeding converters don't seem to be change synchronously.

Input is also offered from totally different renewable energy sources like alternative energy, turbine, cell etc. cell is one in every of the foremost necessary sources of distributed energy attributable to its high potency, high energy density, and high responsiveness and long life as a result of few moving components. Allow us to take into account 2 totally different input voltages area unit given to the 9 level asymmetrical electrical converter we have a tendency to get associate AC output. Since this low level AC output voltage is reborn into high level AC output voltage that's why we have a tendency to area unit exploitation accelerate electrical device. This is often given to the grid of the facility plant. In order to keep up the output quality we have a tendency to use Microcontroller. The Microcontroller is employed to regulate the pulses. This pulse is given to the heart beat generator.

Power-electronic inverters are getting standard for varied industrial drives applications. In recent years conjointly dynamical and medium-voltage drive applications are put in. to beat the restricted semiconductor voltage and current ratings, some quite series and/or parallel affiliation are necessary.

Due to their ability to synthesize waveforms with an improved harmonic spectrum and attain higher voltages, multi-level inverters at receiving increasing attention within the past few years. The structure electrical was introduced as an answer to extend the converter in operation voltage on top of the voltage limits of classical semiconductors. The structure voltage supply electrical converter is recently applied in several industrial applications like ac power provides, static volt-ampere compensators, drive systems, etc. one among the many blessings of structure configuration is that the harmonic reduction within the output undulation while not increasing shift frequency or decreasing the electrical converter power output. The output voltage undulation of a structure electrical converter consists of the quantity of levels of voltages, generally obtained from electrical device voltage sources. The alleged structure starts provides, static volt-ampere compensators, drive systems, etc. one among the many blessings of structure configuration is that the harmonic reduction within the output undulation while not increasing shift frequency or decreasing the electrical converter power output. The output voltage undulation of a structure electrical converter consists of the quantity of levels of voltages, generally obtained from electrical device voltage sources. The alleged structure starts

3. Proposed System

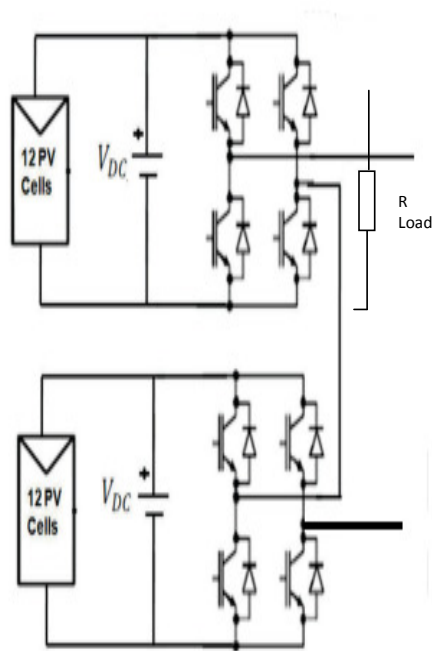


Figure 3.1 proposed circuit

from 2 levels. Because the variety of levels reach time, the output doctor's degree (Total Harmonic Distortion) approaches zero. The quantity of the accomplishable voltage levels, however, is proscribed by voltage unbalance issues, voltage clamping demand, circuit layout, and packaging constraints. Structure inverters synthesizing an outsized variety of levels have plenty of deserves like improved output undulation, a smaller filter size, a lower EMI (Electro Magnetic Interference), and alternative blessings. The principle advantage of victimization structure inverters is that the low harmonic distortion obtained because of the multiple voltage levels at the output and reduced stresses on the shift devices used. Enhancements in quick shift power devices have light-emitting diode to associate magnified interest in voltage supply inverters (VSI) with pulse dimension modulation management (PWM). It's typically accepted that the performance of associate electrical converter, with any shift methods, may be associated with the harmonic contents of its output voltage. Power physical science researchers have perpetually studied several novel management techniques to cut back harmonics in such waveforms. Up-to-date, there are several techniques that are applied to structure electrical converter topologies. Pulse width Modulation (PWM) is wide utilized to manage the output of static power inverters. The rationale for victimization PWM is that they supply voltage and/or current wave shaping made-to-order to the particular

desires of the applying into consideration. It's finally performance and value criteria that determines the selection of a PWM methodology in an exceedingly specific application.

3.2 Need of Asymmetrical Inverter

- Different voltage sources can be used.
- To provide a large number of output levels without increasing the number of inverters, asymmetric multilevel inverters can be used.
- Increasing the number of levels provides more steps; hence, the output voltage will be of higher resolution and the reference sinusoidal output voltage can be better achieved.
- An asymmetrical configuration provides nearly sinusoidal voltages with very low distortion, using less switching devices.
- In addition, torque ripples are greatly reduced
- Asymmetrical multilevel inverter enables a DTC solution for high-power induction motor drives, not only due to the higher voltage capability provided by multilevel inverter.
- But mainly due to the reduced switching losses and the improved output voltage quality, which provides sinusoidal current without output filter.

3.3 Operation of Hybrid Cascaded H- Bridge

The most common multilevel converters, DCMC, FCMC and CCMC, have symmetrical topologies that require redundant states to generate the same voltage levels. When asymmetries are allowed, it is possible to increase the number of voltage levels while reducing the number of components. HCMLI circuit .HCMLI consists of $(n-1)/2$ number of single phase H-Bridge inverters that are connected in series to generate n level of output phase voltage. A single-phase structure of a Single-phase HCMLI with 9 level of output. The output phase voltage is equal to the summation of each H-Bridge module given by the following formula

$$V_0 = V_{m1} + V_{m2} + \dots + V_{mh}$$

Where h is the number of H-Bridge modules used in the multilevel circuit. Each module of H-Bridge has its own input voltage and consists of four switching power devices; S11, S21, S31, and S41. HCMLI has several advantages because its circuit configuration is simple and modular. Each of its modules is identical and incorporates both input and output circuitry. Besides, HCMLI requires the least number of components compared to other types of multilevel inverter. These features provide flexibility in extending HCMLI to higher number of levels without modification on the circuit itself.

4. SIMULATION AND WAVEFORM

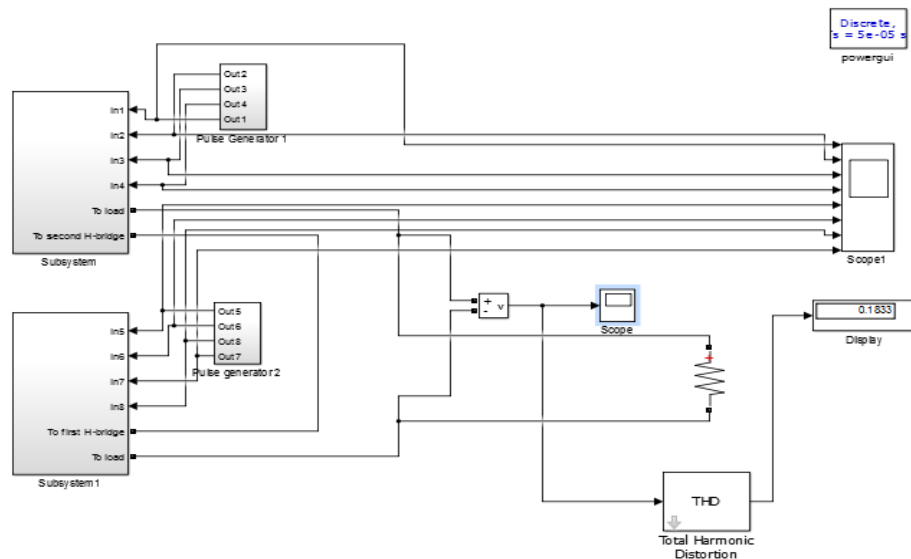
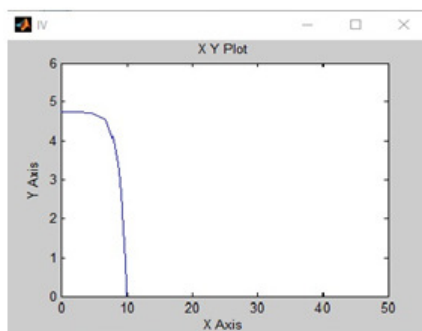


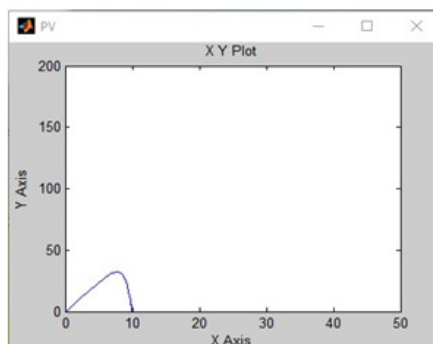
Figure 4.1 simulation diagram of 9 level cascaded H bridge inverter

4.1 Input Waveform

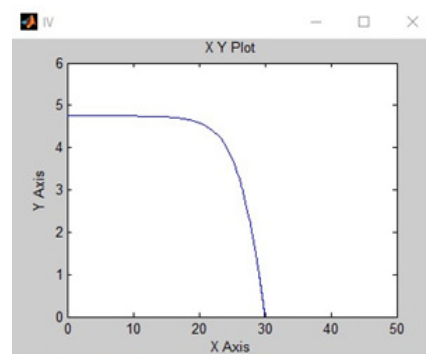
10v wave form



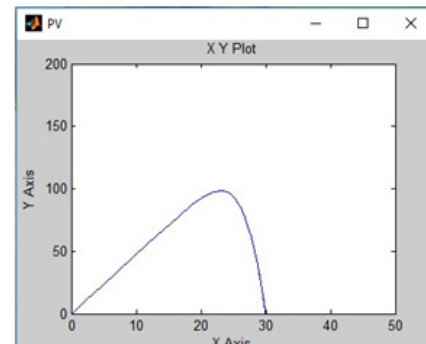
X -Y Plot between current and voltage



X-Y plot between power and voltage
30v waveform



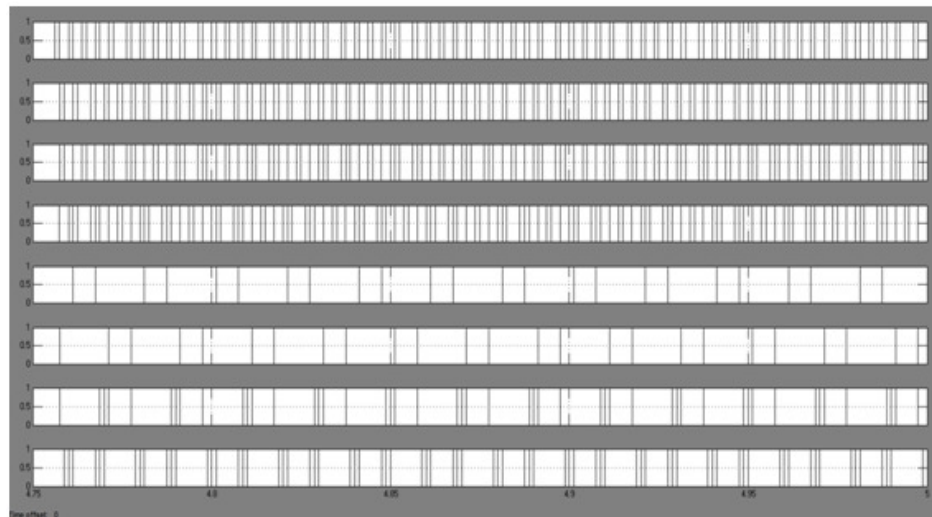
X -Y Plot between current and voltage



X-Y plot between power and voltage

4.2 Output

Output for inverter on-off time



Output for nine-level peak voltage Input voltage of 10v & 30v is given to the cascade h bridge inverter. Both of the positive and negative output voltage levels are generated and the peak voltage is 40v.

5. Conclusion

The total harmonic distortion (THD) = 18.33 percentage level for the inverter voltage. Multilevel electrical converter technology has emerged recently as a really necessary different within the space of high power medium-voltage energy management because of their low switch voltage stress and modularity. The topologies of structure electrical converter have many benefits like lower Doctor of Theology, lower EMI generation, higher output wave shape and better potency for a given quality of output wave shape. Cascaded H-bridge multi-level inverters (CHMLI) square measure a promising breed of multi-level inverters that typically need many freelance dc sources. During this paper the event of PIC microcontroller as an impression circuit for structure single section electrical converter was with success enforced. The simulation output for structure electrical converter was obtained with MATLAB and therefore the same is enforced in hardware exploitation PIC microcontroller and tested. The output from the nine level electrical converter was obtained like the simulated results. In recent years, several multi-level electrical converter of various topologies square measure planned and analyzed so as to scale back harmonic elements of the output voltage and current. If the quantity of level will increase the complexness will increase however the harmonics square measure reduced Speed of switches.

References

- [1] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.
- [2] S. Kouro, M. Malinowski, K. Gopakumar et al., "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, 2010.
- [3] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Mediumvoltage multilevel converters State of the art, challenges, and requirements in Industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010.
- [4] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-PointClamped PWM Inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981.
- [5] T. A. Meynard and H. Foch, "Multilevel conversion: high voltage choppers and voltage source inverters," in *Proceedings of the 23rd Annual IEEE Power Electronics Specialists Conference Record (PESC '92)*, pp. 397–403, June-July 1992.
- [7] F. Z. Peng and J. S. Lai, "Multilevel cascade voltage-source inverter with separate DC source," U.S. Patent 5 642 275, June 1997.

- [8] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-Bridge," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3505–3512, 2012.
- [9] Y.-S. Lai and F.-S. Shyu, "Topology for hybrid multilevel inverter," *IEE Proceedings: Electric Power Applications*, vol. 149, no. 6, pp. 449–458, 2002.
- [10] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 655–667, 2012.
- [11] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET Power Electronics*, vol. 7, no. 1, pp. 96–104, 2014. [11] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched dc sources," *IEEE Transactions*
- [12] T. Padmapriya and V. Saminadan, "Inter-cell Load Balancing Technique for Multi- class Traffic in MIMO - LTE - A Networks", *International Conference on Advanced Computer Science and Information Technology*, Singapore, vol.3, no.8, July 2015.
- [13] M. Rajesh, Manikanthan, "ANNOYED REALM OUTLOOK TAXONOMY USING TWIN TRANSFER LEARNING", *International Journal of Pure and Applied Mathematics*, ISSN NO:1314-3395, Vol-116, No. 21, Oct 2017.

