

Analysis of CAM cell for minimum number of transistor count

Arulpriya.S¹, Arun.A²

AP/ECE,

M.Kumarasamy College of Engineering,

Karur, TamilNadu

arul.priya91@gmail.com, aruna.ece@mkce.ac.in

Abstract— Content Addressable Memory is a technique to search the memory location by giving a data. Parallel search operation in the case of CAM can reduce the access time but the power and the area consumption is more. Normally the CAM consists of the priority encoder and the sensing circuit where in the encoder performs the operation with less energy. Total area utilized by the CAM is oriented on SRAM alone. In this paper the idea of designing the SRAM with different number of transistor count can be analyzed. The power consumption and the area can reduce to a specified value.

Keywords—Content addressable Memory(CAM), Static Random Access Memory, Match Line(ML), Search Line(SL)

I. INTRODUCTION

Random Access memory(RAM) is mainly used for storing the data. In this the data can be read or write roughly with same amount of time regardless of the order of the data. In direct access data storage media, the time required read and write operation can be varied based on the location where the data has to be stored due to some mechanical limitations. RAM is volatile memory there is some challenges while it is designed as non-volatile such as write operation cannot be performed randomly.

II. OVERVIEW OF CAM CELL

There are several ways of representing the single bit CAM cell. It can be designed using either NAND or NOR or combined design as NAND-NOR implementation. But the drawback behind all those above mentioned method is that n-bit CAM can require a precharge phase, to make the match line stay at logic of high level. It also having an evaluation phase (eval), in this phase match line getting discharged when the match does not occur, either through a driven transistor NMOS in the NAND-based CAM or through the NOR cells in the NAND-based CAM. To rectify the problems stated above, a new CAM cell design has been implemented, that is based on the XOR function, instead the NAND and NOR functions. Already the XNOR based CAM has been come across but still now not yet reach the world properly. Previously the CAM cell with XNOR function can be implemented using 4 NMOS pass transistors. But the XOR function now being implemented by the complementary pass transistor. The new design is going to concentrate in the

reduction of transistor, power reduction and the robustness. The new cell XORAM, consists of a 6T SRAM and the XOR gate.

Here the SRAM cell contains both the bit (A) and the inverse bit ($\bar{A}$). Another important point is that the XOR gate can be designed using four MOS transistors and we obtain the cell as fig.4

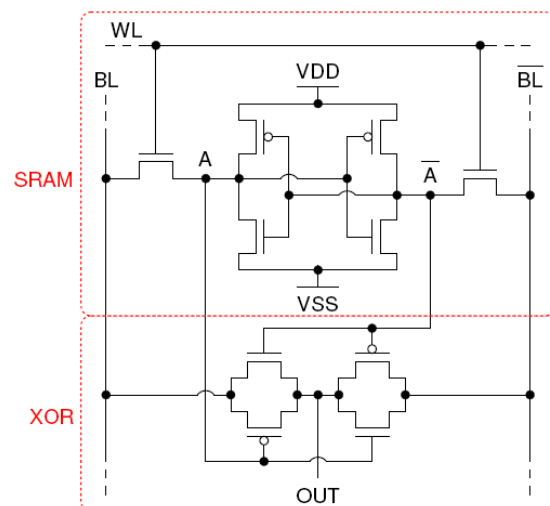


Fig.4 XORAM based single CAM cell

In the above diagram the SRAM can be used to read / write operation and the output is connected to the XOR cell where the output is generated according to the input given. For example both the bit and the inverse bit are different then automatically the output of XOR is '1' otherwise it becomes '0'. Based on this the search word matches with the stored word or not can be finalized. This XORAM based CAM cell contains the 6T transistor SRAM. This SRAM cell can be analyzed and designed using 4T and 2T MOS transistor.

II. REVIEW ON SRAM

A. 6T SRAM CELL

SRAM is designed using two cross coupled inverter in which the data is stored. It is used mainly in microprocessor, mainframe computers ,etc. for cache memory. SRAM is a bistable device consisting of two back to back inverter(M1,M2,M3&M4) along with the access transistor(M5&M6) that too separately connected to complementary bit lines b & b bar. The internal node can be accessed by using the access transistor. Here two stable states are considered state '0' & state '1'. SRAM uses the Latch and it is static in nature so that the data can be kept as long the power is turned on, it does not require any refresh.

BASIC OPERATION

In SRAM there are three modes of operation that is standby(hold) mode, read mode and write mode

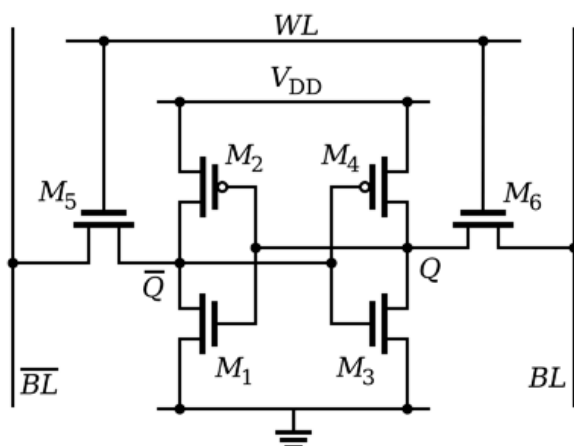


Fig 1. 6T SRAM Memory cell

A. Standby mode (Idle circuit)

In this the word line $WL = 0$ so that the transistors M5 and M6 connected to the cross coupled inverter is in off condition. The cell cannot be accessed during this condition. The data in the inverter M1 and M3 will be feedback until it is connected to the supply and the data is retained in the memory. In SRAM array most of the cell are in the standby mode.

B. Read Mode

In read mode the bit lines b and b bar can be precharged to the high value. Now the $WL=1$ enables the transistors M5 and M6. So that the data stored in the point Q and Qbar are connected to the b and b bar respectively. For example '1' is stored in Q then the transistor M1 drops to '0' and at the same time M4 charges to VDD, the stored value can read by the user easily. The voltage difference between two states are very small which has to be given to the sense

amplifier so that the low voltage is taken as '0' and high voltage is taken as '1'.

C. Write Mode (update of data)

In write operation, the external driver is needed to activate, then only the previous state of the cross-coupled inverter can be easily over write. Now the WL is enabled and the data to be written into the cell is given in the bit line b and b bar. The data to be written is n'0' in the place of '1'. Once the bit line data reaches the input of the cross coupled inverter, the current starts to flow through the pull ups to the bit line through the storage node storing high, turned to '0'. If same data has to be store then there is no change occurs.

B. 4T SRAM

In 4T SRAM design as shown in fig.2, a pair of PMOS and NMOS that will form a twisted inverter and the access of data can be done through two NMOS transistor. The inverter is having one NMOS to work as a driver transistor and PMOS acts as load transistor. Not like a 6T cell it requires two inverter having a pair of NMOS and PMOS and a pair of NMOS to do read and write operation. In 4T SRAM reading and writing can be done separately on each node. A feedback is employed between two nodes, the new data can be transferred into the cell using WL line. Similar to 6T, reading and writing operation can be performed in 4T SRAM cell also but the data storage alone in STB node instead of ST node. When write operation is carried on complement of data is placed on STB node and in ST node opposite data has to be placed, data transfer to ST and STB node starts when the access transistor is turned ON by the WL line.

The data to be written is '0' automatically ST node discharged to ground by the driver transistor and STB node charges to VDD using load transistor. When '1' has to be written into cell load and driver transistor is OFF condition. The threshold of each transistor has to be adjusted for retaining the data without giving any refresh cycle. Here the precharge to supply voltage on BL and BLB line is carried out during write operation. Charge on ST and STB node is now discharged through BL and BLB line. Difference voltage BL and BLB is sensed by sense amplifier and data can be read through the output of the sense amplifier.

To read '0', voltage on ST node should be low then the access transistor will pull down the voltage on BL. When SE signal goes high that will enable sense amplifier and read data '0'. To read '1' opposite process that is BL and ST node should have same voltage and the data can be read in sense amplifier output.

C. 2T SRAM

A newly proposed SRAM cell from fig.3 having only 2 transistors. In this cell NMOS acts as a driver transistor and PMOS acts as a load transistor. Data storage can be done at the interconnection of both transistors at Q. Here the driver transistor will itself acts as access transistor also. During read

and write cycle access can be done by using WL line which in turn is connected to gate input of NMOS. Here the bit line used is only single not like 6T and 4T SRAM cell which uses 2 Bitline. Automatically precharge and sense amplifier is also

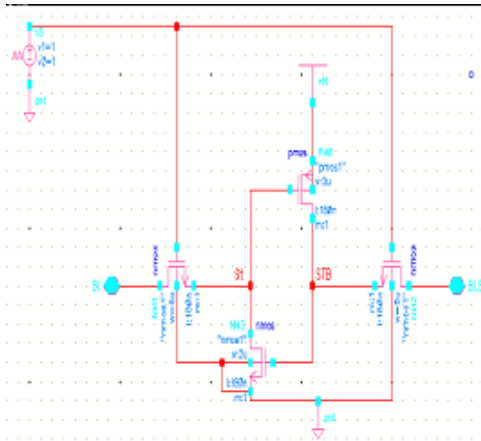


Fig 2. 4T SRAM cell

single ended. To determine the output in sense amplifier, the charge stored in BL will drive the sense amplifier. Cell area can be reduced.

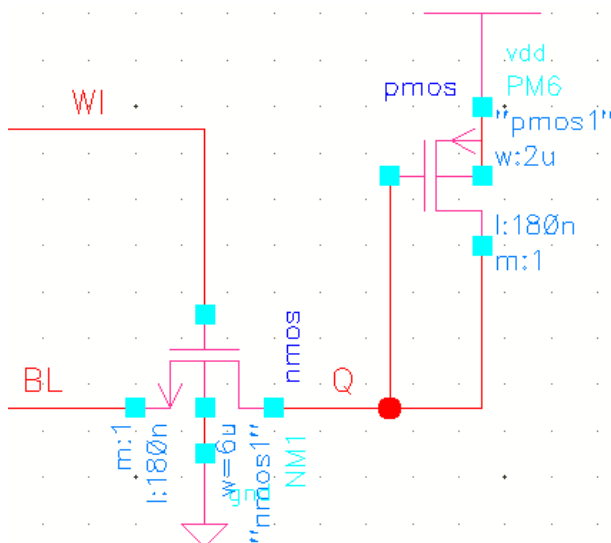


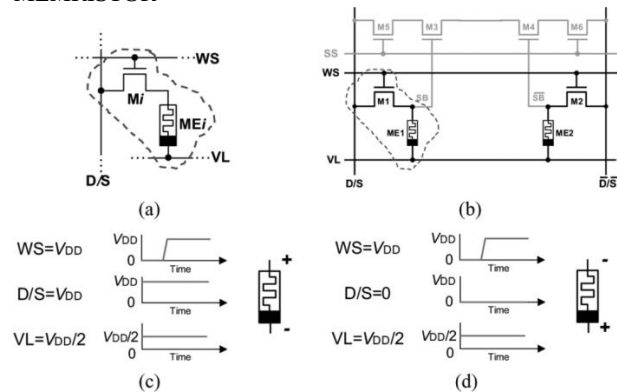
Fig 3. 2T SRAM cell

Driver transistor assist to write the data which is to be placed on BL. If the data to be written is "1", Q can be charged to maximum value through access transistor which turns on by WL. If data to be written is "0", there occurs a direct path to ground from node Q and discharges through driver transistor. Load transistor also discharges to ground to maintain low voltage at node Q. In order to obtain the width of the driver transistor to be three times higher than the load

transistors. Read cycle can be performed through sense amplifier.

D.MEMRISTOR NMOS CIRCUIT

Here the storage cell uses a logic "1" for writing, the memristor receives a positive bias to maintain an "ON" state. This corresponds to the memristor being programmed as a logic "1." To program a "0" a reverse bias is applied to the memristor, which makes the memristor resistance high. This corresponds to logic "0" being programmed. The fig shows the MEMRISTOR



III.RESULTS AND DISCUSSION

The area of the SRAM can be comparatively reduced for 2T and it can be approximately 65% reduction. Now a days the CAM cell is focused on 6T logic alone. In future this can be implemented by using 4T logic or the 2T logic further reduction in area of the CAM cell can also be possible. Another thing to be focused is the power in case of 2T logic since the power needed for 2T logic is more.

S.No	SRAM cell	Avg power
1	6T	922.7uw
2	4T	64.74uw
3	2T	59.24mw

Table I: Comparison of power in various SRAM

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