

N-DETECT TEST SETS: A NOVEL APPROACH FOR LFSR FAULT SIMULATOR ANALYSIS USING VLSI CIRCUITS

¹Ezhilarasi V., ²Santhosh P., ³Priyadharshini S

^{1,2,3}Assistant Professor, Karpagam College of Engineering, Coimbatore, Tamilnadu, India.

¹ezhilarasivijaykumar@gmail.com, ²santhosivam@kce.ac.in

³priya.maha.it@gmail.com

Abstract: Identifying the faults in the electronic circuits is a hard process. Hence, detecting a flaw more than one time has high degree of fault coverage. Previous works shows that n-detect test sets are of increased quality for a number of common defects. Method for multiple detect test generation usually produce fully specified test vectors. These fully specified bits increase the complexity of the test process. In order to avoid this, this paper goes in for a new technique of increasing the unspecified bits so as to minimize the compactness of the vectors that is used (usage of n-detect relaxed algorithm). S27 Benchmark circuit is used to analyze the process, where single Stuck-at-faults are introduced arbitrarily and the test process is carried out using 4- bit sequence pattern of 16 combinations. These patterns are generated randomly by using LFSR. The patterns that are generated, flow through the entire circuit, and compare it with the faults that are present in the components, either at the input or output. During the comparison if the component response and the pattern response are same, then it is considered as a fault free component. If the response differs, they are considered as fault and are recorded. In this manner many patterns detect the same faults or different faults. The patterns that detect the same faults are grouped together and are reduced into single pattern with unspecified bits which is denoted by 'x'. These unspecified bits are obtained by comparing these patterns, in bit wise manner. We use saboteurs and mutant techniques for test pattern reduction and comparing the output with relaxed n-detect test set. This process can be clearly demonstrated by using MODEL SIM 6.3f and Xilinx ISE 9.2isimulator.

Index Terms: ATPG, LFSR, Relaxation, Saboteurs, Mutants, Digital Circuit testing (DCT).

1. Introduction

All VLSI manufactured chips are tested for identifying defects. Defects are modeled as faults to ease the test pattern generation process. Among the various fault models, stuck-at fault is widely accepted because of its

closeness in detecting the faults. Advanced techniques are used, which make the process highly complex.

n-detect test pattern generation and compaction technique produce test sets that are full specified (i.e., test bits have a fixed value of 0 or 1), and these specified bits are decreased gradually, while maintaining its overall fault coverage. Flexible test sets are also extremely used in low power test vector generation techniques like those in [3] and [4]. Simulation-based fault injection method [1]-[2] is a useful way to estimate the dependability of a system during the design part, thereby reducing the time-to-market [6]-[8]. Saboteurs and Mutant component are introduced in the circuit level to analyze the performance of test patterns in detecting the faults. The fault is injected using a dependability validation technique which is based on the realization of the controlled experiments where the observation of the circuit behaviour in presence of faults is obviously induced by the deliberate introduction of faults into the system.

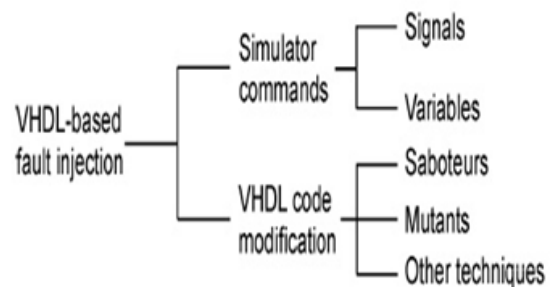


Figure 1. Types of fault injection methods

A. Saboteurs

A saboteur is a special VHDL component added to the original model.[9] When started, the work of this component is to modify the value, or timing characteristics, of one or more signals, simulating the occurrence of a fault.

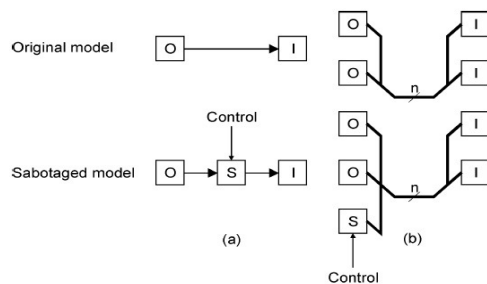


Figure 2. Types of saboteurs(a) Serial.(b) Parallel

B. Mutants

A mutant is a component that replaces another component. When it's inactive, it works like the original component, but when initiated, it works like the component in presence of faults. Mutation Analysis (MA) is a fault detection based simulation approach that is used to measure the quality of test benches for mutant detections

The mutation can be made in three ways:

- (i) By adding saboteurs to structural description.
- (ii) By modifying structural descriptions replacing sub-components(a NAND gate can be replaced by a NOR gate)
- (iii) By modifying syntactical structures of behavioral descriptions.
- (iv)

2. Methodology

A. Fault Modeling

It is not possible to enumerate all the physical defects and develop tests cases for the defects which are modeled as faults. These fault models emulate the behavior of physical defects while simplifying the test generation process. Logical fault models may be structural and functional. Structural fault models are of stuck at fixed logic and bridging faults. Of the various fault models, stuck-at fault model is widely accepted because of its closeness in detecting the defects and its simplicity in generating test vectors. Various efficient algorithms have been developed and programmed to powerfully generate tests for single stuck-at faults. LFSR which generates the test patterns find out these faults by comparing the generated test patterns with the original circuit output pattern before fault injection method. By using this concept we are able to describe the faults connected to a component. For the conclusion that the mean time between faults and their duration would be integral part of the description of each behavioral component of the model. In order to demonstrate the viability of this procedure, we developed the verification tool which allows the integrated description of the fault free behavioral as

well as the component's behavioral after one of the faults correlated with this component has been activated.

B. Shift register

LFSR is a sequential shift register whose input is a linear function of its prior state. The most frequently used linear function of single bits is XOR. It is driven by exclusive-or of some bits of the overall shift register value. The first input for the LFSR is referred as the seed. The group of values generated by register is purely identified by its current or previous state. Similarly, because the register has a fixed number of probable states, it must eventually enter a repeating cycle. LFSRs are used in testing, for pattern generation. Some of the applications in data compression, Built-in Self-Test, optimized counter, digital signal processing.

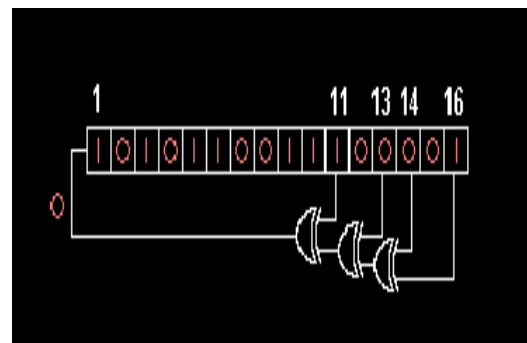


Figure 3. Linear Feedback shift register

C. Pattern Generation

The ATPG technique SCARLETT (Self-testCode Ableand Reduced Length Test Tool) is provided which is particularly mapped for the BIST scheme. ATPG procedure which involves generation of input patterns that are used for checking existence or absence of faults(s) at some location in a circuit. The proposed technique is applied to the hard-to-detect faults remaining after a pseudo-random sequence of length and minimizes the storage requirements for the resulting deterministic test set. The proposed algorithm supports the linking of patterns. Test patterns are generated until the limits for a group of patterns to be concatenated are reached. All patterns in this group clubbed as one pattern which is encoded as a initiator for one of the available polynomial and the first bit of the LFSR chain resulting from this seed are determined. Since this subsequence refers to the fully specified patterns that is fed into the scan chain during test mode it is fault simulated against the remaining fault set. Faults that are detected along with the existing target

faults can be dropped immediately and the process is repeated.

D. n-Detect Tests

n-detect tests are considered to be stuck-at fault tests where each stuck-at fault is detected at least n times by n different test vectors. It is observed that the n-detect tests gives a better fault coverage than single-detect stuck-at fault tests[4][5]. Identifying the same single stuck-at fault under various excitation and observation conditions enhances the chances of finding different bridging faults. Various test generation strategies have been developed to generate efficient n-detect tests.

E. Pattern Minimization

A new approach is designed based on the characteristics and parameters of the n-detect test sets. A novel systematic test switching algorithm is schemed in which each test is replaced by a new one that detects a subset of the faults detected by the first one with fewer specified bits. The algorithm explicitly removes additional detections for each fault. Thus it selects the “best” tests to detect the fault and drops the fault from the remaining tests in order to minimize the total number of specified bits in these tests. A simple X-filling method for low power testing has been used in order to illustrate how relaxed test sets can benefit low power testing. An example illustrating the proposed method's execution is presented gives the obtained experimental results for the specified bits reduction as well as the outcome of the proposed method in X-filling for low power test. This experimentation was done using the popular stuck-at model. Fig 5 shows the flow process of proposed method.

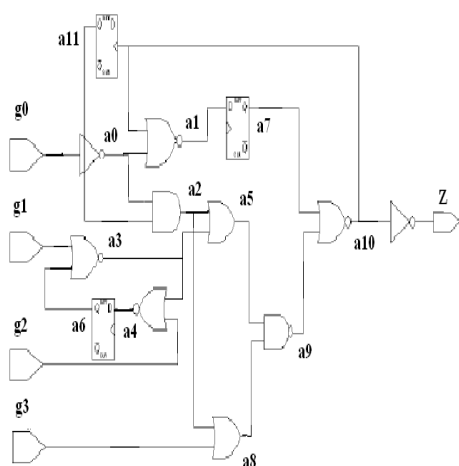


Figure 4. s27 Benchmark circuit

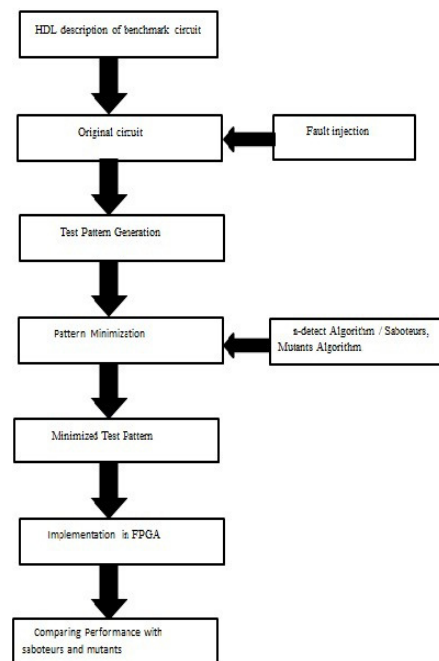


Figure 5. Flowchart for Test Reduction Techniques

3. Experimental Results

The proposed algorithm was implemented using vhdl in Model sim and is linked with Xilinx 9.2i. All experiments were run on Spartan 3E FPGA versions of the ISCAS'89 benchmark circuit(s27 circuit). In this paper, we first described about test generation of n-detect test set in the fig 4, which is of great importance. This method generates a optimized test pattern which identifies a particular set of faults and holds a small number of specified bits. This procedure can be implemented using either a structural-based or a functional-based test pattern manipulation framework without affecting the effectiveness of the fault coverage. Fig 7 shows test pattern reduction by using X-Filling algorithm.

Fig 8 describes the test pattern reduction using Saboteurs and mutants. Fig 9-12 shows number of hardware required for implementing in FPGA and power consumed in the overall process which is obtained from Xilinx estimator(XE). Finally both the techniques are compared and it is depicted in table 1 and it is notified that test vectors efficiently reduced from 16 test vectors to 5 test vectors in relaxed n-detect test set. Timing required for getting the output is comparatively less. Power plays vital role in the VLSI technology which is even handled good and number of hardware to implement in the form of gates is less.

A. Simulation Result



Figure 6. Test pattern Generation

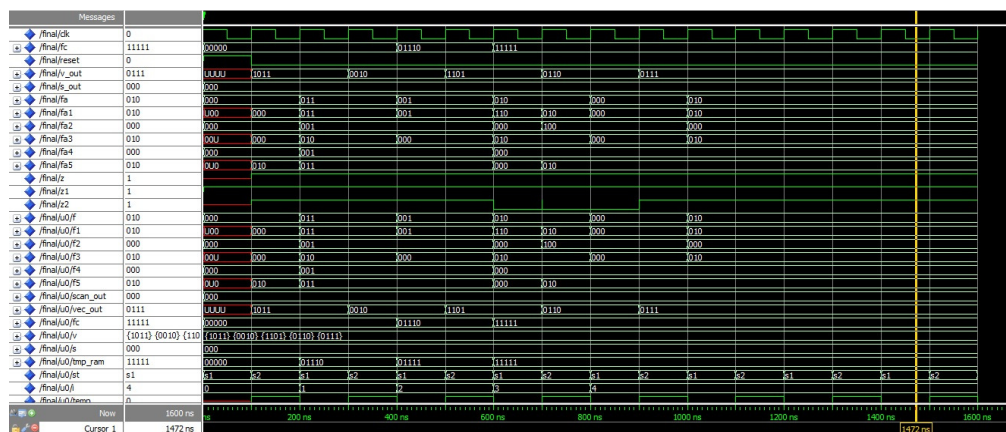


Figure 7. n-detect test set

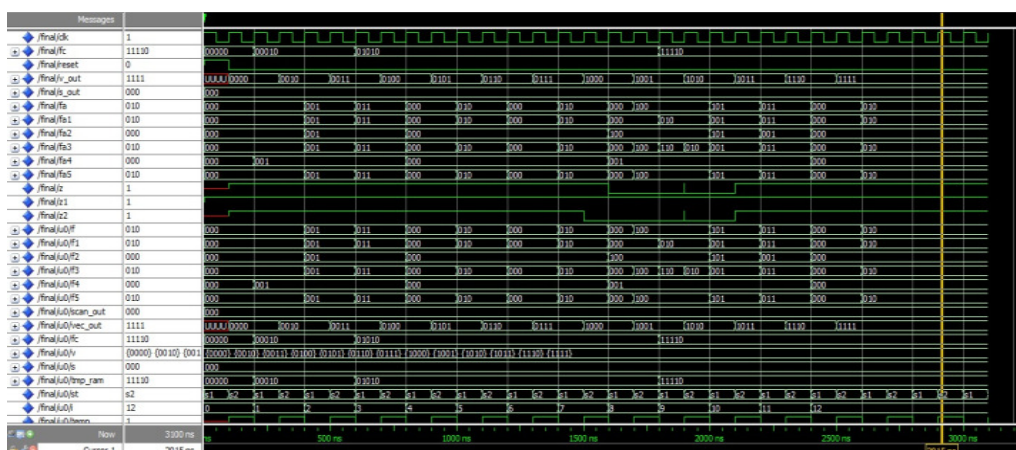


Figure 8. Saboteurs and mutants

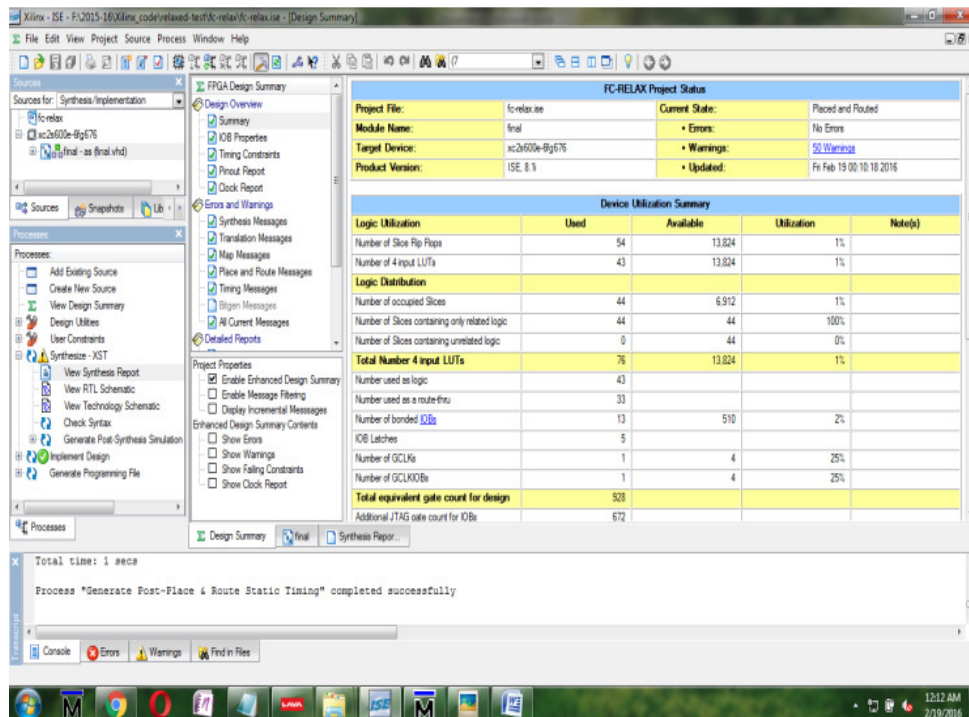


Figure 9. Gate count for relaxed test set

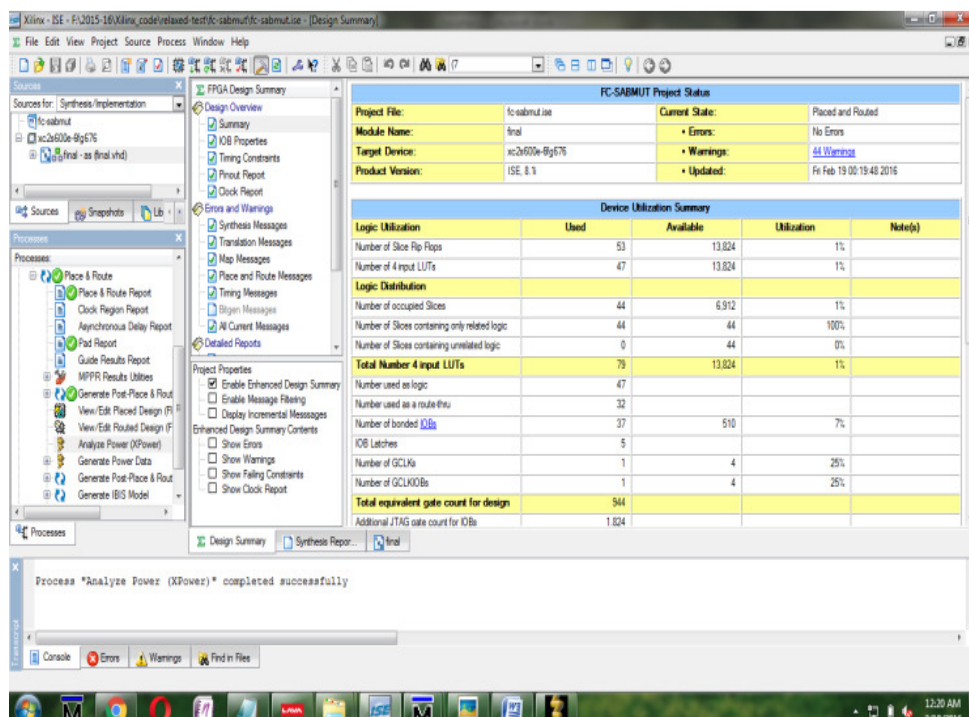


Figure 10. Gate count for Sub-mutant

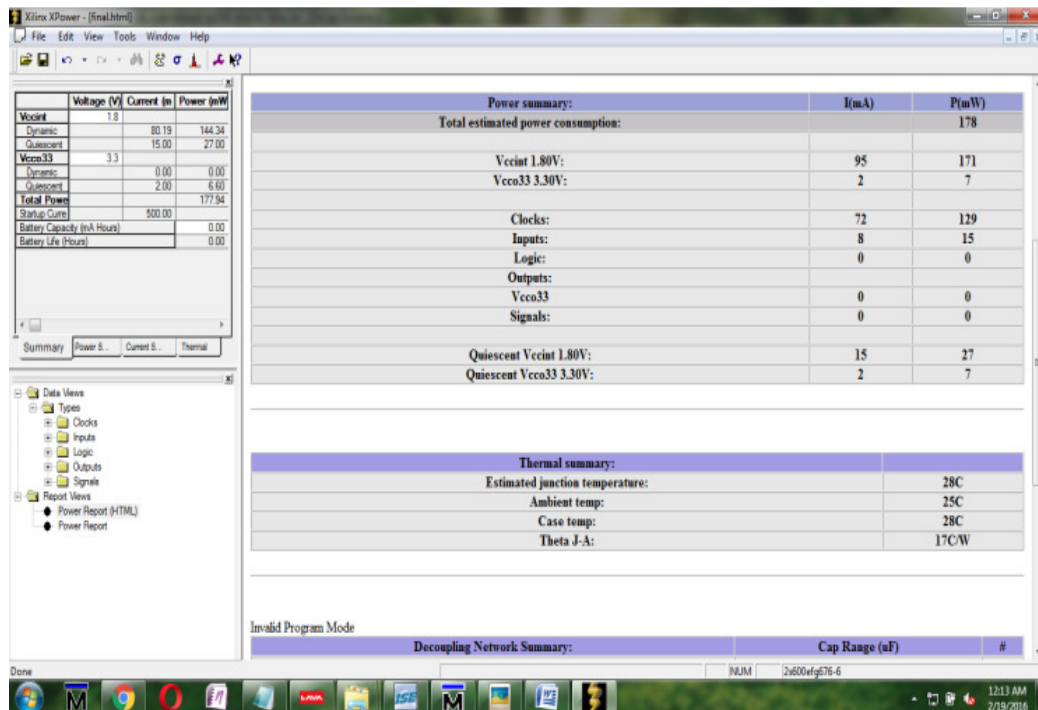


Figure 11. Power report for relaxed test set

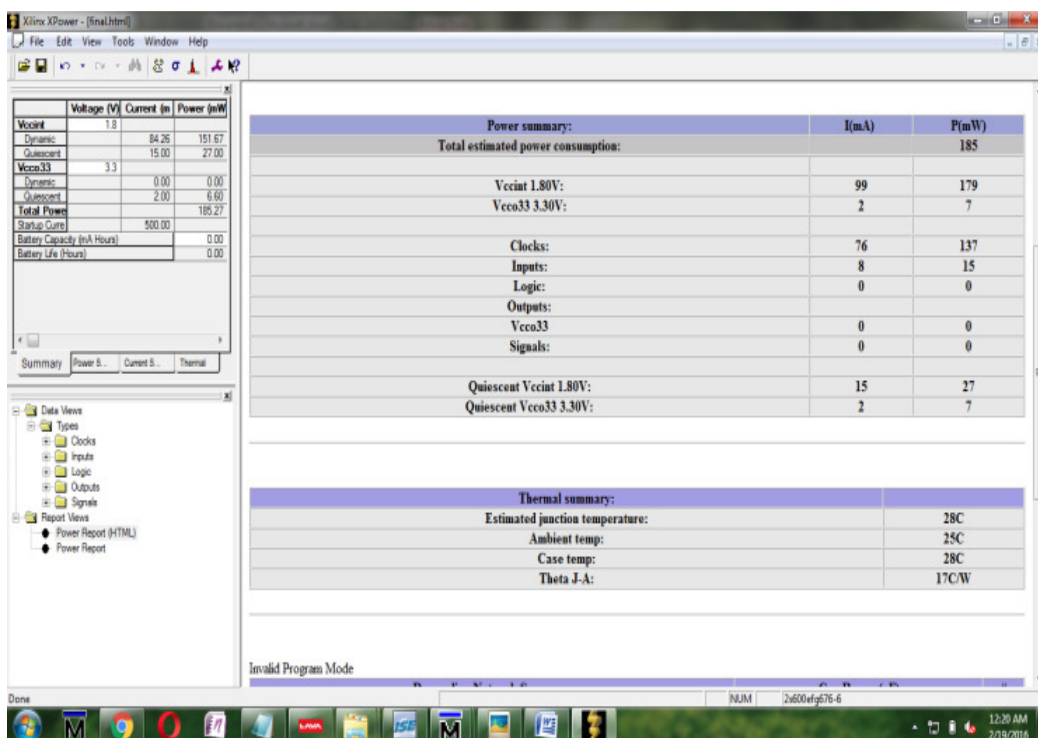


Figure 12. Power report for Sub-Mutant

Table 1. Relaxed n-detect test set

TEST VECTOR REDUCTION			
n1	1011	1011	1XX1
n2	0010		
n3	0010	0010	0X10
n4	0110	0110	
n5	0111	0111	
n6	1011	1101	0111
n7	1101		
n8	1101		

Table 2. Performance of various techniques

SPECIFICATION	n-DETECT TEST SET	SABOTEURS AND MUTANTS
Reduced Test vectors	5	12
Maximum output required time after clock	8.394ns	10.820ns
Total equivalent gate count for design	928	944
Clock pulse required	72	76
Total estimated power consumption	178mW	185mW

4. Conclusion

The test pattern is minimized by investigating the impact of test set relaxation in n-detect test sets. A systematic methodology for decreasing the number of specified bits in a given n-detect test set or a multiple detect test set. The results obtained from the experimental analysis visualize the credentials of the above implemented method in achieving high specified bit reduction rates in n-detect test sets while maintaining the n-detect fault coverage. Provided the discussions and experimental data states the similarity before the application of relaxed test sets. Thus by using MODEL SIM 6.3f and Xilinx software we are able to prove that the compactness of the test patterns that has been applied to the S₂₇ circuit. Test Data compression is done well and good in relaxed n-detect test set comparing to other fault injection techniques, as a future work both the methods are implemented in FPGA and we can find the performance of CPU efficiency.

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