DESIGN AND ANALYSIS OF POWER EFFICIENT FULL ADDER IN 30NM TECHNOLOGY

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Abstract: Adiabatic circuits and standard CMOS (Complementary Metal Oxide Semiconductor) logic are widely employed in low power VLSI (Very Large Scale Integration) chips to achieve high system performance. The power saving of adiabatic circuit can reach more than 90% compared to conventional static CMOS logic. When adiabatic switching is used, the signal energies stored on circuit capacitance may be recycled instead of dissipated as heat. This paper mainly concentrates on the design of FULL ADDER based on adiabatic switching principle that uses a pair of complementary split-level sinusoidal power supply clocks for digital low power applications. Comparing to other standard adiabatic logic styles the proposed 2PASCL (Two Phase Adiabatic Static Clocked Logic) adiabatic logic holds better power result. The simulation is carried out in SYNOPSYS EDA software at 30nm technology for different frequency range.

Keywords: Adiabatic logic, Full Adder, ECRL, PFAL, 2PASCL, power dissipation.

1. Introduction

The importance of reducing power dissipation in digital systems is increasing as the range and sophistication of applications in portable and embedded computing continues to increase. With the widespread use of mobile, hand-held and wireless electronics devices, the demands for the innovations of low power VLSI arise. For most of the digital circuits today, CMOS logic scheme has been the technology of choice for implementing low-power systems [1].

Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy. In ideal adiabatic logic, each charge could be recycled (reused) an infinite number of times. So that a significant power dissipation reduction would be possible [4]. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. There are some classical approaches to reduce the dynamic power such as reducing supply voltage, decreasing physical capacitance and reducing switching activity [13].

The power supplies of adiabatic logic circuits have also used circuit elements capable of storing energy. This is often done using inductors, which store the energy by converting it to magnetic flux, or using capacitors, which can directly store electric charge. Because of the reversibility requirements for a system to be fully adiabatic, most of these synonyms actually refer to, and can be used inter-changeably, to describe quasi adiabatic systems[4].

Adiabatic logics are of two types. They are:

Partially adiabatic logic: It is a logic having non-adiabatic Loss present i.e. there is non-zero VDS across transistor when it is being turned ON. It doesn’t depend upon frequency.

Fully adiabatic logic: It is a logic having non-adiabatic loss Absent.

The different partially adiabatic logic such as efficient charge recovery logic circuit (ECRL) and Positive Feedback adiabatic logic (PFAL) is implemented to design full adder circuit under 30nm technology in this paper. The design of Low power Full Adder circuit using 2PASCL adiabatic logic is proposed in this paper.

This paper is organized as follows: section II discusses the ECRL, PFAL adiabatic logic and proposed design-2PASCL adiabatic logic for full adder circuit. Section III describes the simulation part of the proposed design. Section IV concludes the paper.

2. Design of Different Adiabatic Logic Structure

The two different partially adiabatic logic structures and the proposed adiabatic logic is implemented in full adder circuit.
A. Efficient Charge Recovery Logic (ECRL)

The conventional ECRL is shown in figure 1. It consists of two cross-coupled transistors M1 and M2 and two NMOS transistors. An AC power supply power is used for ECRL gates, so as to recover and reuse the supplied energy.

Both out and /out are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal [3].

![Figure 1. Schematic Diagram of ECRL](image1)

Each power-clock cycle as shown in figure 2 consists of four intervals. In the evaluate (E) interval, the outputs are evaluated from the stable input signals. During the hold (H) interval, outputs are kept stable. Energy is recovered in the interval called recover (R). And for symmetry reasons, a wait (W) interval is inserted, as symmetric signals are easier and more efficient.

![Figure 2. Scheme of the four phase power clock](image2)

B. Positive Feedback Adiabatic Logic (PFAL)

The next adiabatic logic considered is Positive Feedback Adiabatic Logic shown in figure 3. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3 M4, that avoids a logic level degradation on the output nodes out and /out. The two n-trees realize the logic functions [3]. This logic family also generates both positive and negative outputs.

![Figure 3. Schematic Diagram of PFAL](image3)

C. Two Phase Adiabatic Static Clocked Logic (2PASCL)

The proposed 2PASCL is shown in figure 4. The main difference between proposed circuit and static CMOS logic gate is the two diodes, one from the output node to the power clock supply and another one is placed next to the NMOS logic to another power clock. Both MOSFET-diodes are used to re-cycle the charges from the output node, to improve discharging speed of internal signal nodes.

![Figure 4. Schematic Diagram of 2PASCL](image4)
The power dissipation in the Two Phase Adiabatic Static Clocked Logic circuit can be reduced by controlling the peak current through the transistors during charging and discharging [5].

The AND gate is designed using 2PASCL adiabatic logic in Synopsys-Custom Designer tool under 30nm technology as shown in figure 4. Here two sinusoidal power clocks are used, which are out of phase. During the evaluation phase of the power clocks, the potential difference is maximum between the clocks and load capacitor is charged up to peak and output is obtained [4]. In the hold phase of the power clock, the charge from capacitor is recovered. In this way energy is recovered from the output node.

**D. Full Adder using 2PASCL Adiabatic logic**

The proposed design is full adder circuit under 2PASCL adiabatic logic technique consumes less power while comparing to the other adiabatic logic technique and holds good result.

The design of proposed full adder is designed using custom designer of SYNOPSYS tool under 30nm technology is shown in 5. The proposed design is simulated for different range of frequencies and examined for the total power dissipation.
The above full adder circuit was designed using two half adder circuit under 2PASCL Adiabatic Logic technique, mainly used to reduce the power dissipation of the circuit. The power reduction is mainly due to two sinusoidal power clocks which are out of phase [5]. The full adder circuit designed using the partially adiabatic logic holds high power while comparing to the proposed system.

The one-bit full adder used is a three-input two-output block. The inputs are the two bits to be summed and the carry bit, which derives from the calculations of the previous digits [10]. The outputs are the result of the sum operation and the resulting value of the carry bit. Here the full adder designed using two half adder circuit and or gate where these circuits are converted into the cells and each half adder block consist of EXOR and AND gate, the OR gate cell is designed using CMOS logic. The output sum and carry is given by:

\[
\text{SUM} = A \oplus B \oplus C \\
\text{CARRY} = AB + BC + CA
\]

3. Simulation Results and Performance Evaluation

Power is considered as the most important parameter for designing circuits in VLSI. The power consumption of the full adder circuit using Partially Adiabatic logic techniques (ECRL & PFAL) is considered [9]. So the proposed low power full adder circuit using 2PASCL adiabatic logic technique has an optimized power for various frequencies.
Table 1. Comparison of Power Consumed by Full Adder Circuit Designed using various Adiabatic Logic under 30nm Technology

<table>
<thead>
<tr>
<th>DESIGN/ FREQUENCY</th>
<th>100MHZ</th>
<th>400MHZ</th>
<th>800MHZ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full adder using ECRL</td>
<td>25.67mw</td>
<td>27.9mw</td>
<td>29.34mw</td>
</tr>
<tr>
<td>Full adder using PFAL</td>
<td>15.1mw</td>
<td>18.89mw</td>
<td>20.34mw</td>
</tr>
<tr>
<td>Full adder using 2PASCL (proposed design)</td>
<td><strong>8.24mw</strong></td>
<td><strong>9.54mw</strong></td>
<td><strong>12.9mw</strong></td>
</tr>
</tbody>
</table>

Figure 6. Output waveform of the full adder Circuit using 2PASCL adiabatic logic with 100MHZ frequency
Figure 6 illustrate the output waveform of the full adder circuit using 2PASCL adiabatic logic with 100MHZ frequency and also describe the power consumed by the input and output terminals. The average power consumed by the design is about 8.24mw.

Figure 7 illustrate the output waveform of the Full Adder Circuit using 2PASCL Adiabatic Logic with 400MHZ frequency and also describe the power consumed by the input and output terminals. The average power consumed by the design is about 9.54mw.

Figure 7. Output waveform of the Full Adder Circuit using 2PASCL Adiabatic Logic with 400MHZ frequency
Figure 8 illustrate the output waveform of the full adder circuit using 2PASCL adiabatic logic with 800MHZ frequency and also describe the power consumed by the input and output terminals. The average power consumed by the design is about 12.9mw.

4. Conclusion

This paper has described a simulation of power efficient FULL ADDER based on 2PASCL adiabatic logic.

By implementing the adiabatic charging and energy recovery theory, the proposed circuit gives the lowest result in power dissipation of all the simulated adiabatic FULL ADDER. The power dissipation measurement by SYNOPSYS CUSTOM DESIGNER proved that this approach lowers the power dissipation. The design principle can also be used for designing more complicated adiabatic CMOS circuits and its logic schemes for ultra-low energy computing.
References


