Quantum Dot Cellular Automata (QCA) based 4-Bit Shift Register using efficient JK Flip Flop

Birinderjit Singh Kalyan ¹ and Balwinder Singh²
¹ I K Gujral Punjab Technical University, Jalandhar, Panjab, India. birinderjit@msn.com
² Centre for Development of Advanced Computing (C-DAC), Mohali, India. balwinder@cdac.in

January 25, 2018

Abstract

Abstract: The Quantum-dot Cellular Automata (QCA) is a replacement of the conventional CMOS technology for nano computing devices. This technology aids to achieve extra low power, lower complexity sequential structures with very high speed. In this paper JK flip flop is redesigned and compared with previous structures. The JK flip flop based QCA structure which has 78% lesser complexity and covered 66.6 % less area with half latency than previous designs. Further the novel 4 bit shift register was designed as well as simulated in QCA designer tool using proposed JK flip flop. The total area covered by shift register is 0.20 μm² with single clock cycle delay. The power estimation is done in QCAPro tool.

Key Words: Quantum Cellular Automata (QCA); Majority gate Logic; Flip Flop (FF); Sequential Logic; clock (Clk); QCA Designer.
1 INTRODUCTION

The nano-computing [2] is becoming more popular by nature due to its high speed and lower complexity for implementation. This technology leads to more complex structures which were first of all proposed by Lent et al [1]. The QCA cell is the building architecture of any circuit from which the basic gates and logic devices are designed. The research involves first at the physical level and then to the simulation tool which is QCA Designer tool introduced and various test were reported [3-5]. The QCA technology has many advantages as its high operational speed, low-power consumption and lower complexity [6-9]. In this paper the JK flip flop using QCA cells are redesigned and effectively used to realize more complex sequential circuits like shift register. In the basic of QCA, the schematic figure 1(a) shows the QCA nanostructure with four quantum dots which have placed at the square boundary corners. This quantum cell comprises of twin electrons those can tunnel through these four quantum interstitial positions at the corner of the square cell. Tunneling doesn’t happen between the two adjoining corners. The Quantum dots (denoted as i) in the cell where i=1, i=2, i=3 and i= 4 represent the different interstitial positions of dots. The polarization P in a cell can be explained by equation 1, where ρ is the polarization positions in QCA cell.

\[
P = \frac{(\rho_1 + \rho_2) - (\rho_3 + \rho_4)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)}
\]

The polarization comprises the different charge configuration that will define the various logics which is distributed among four dots. Likewise, the polarization is -1 when i=4 and i=2 are at higher state and polarization become +1 when i=3 and i=1 at higher state. Binary information is also represented in QCA by figure 1(a) in the forms of logics.
Due to coulombic repulsion [1], the cell occupies the antipodal sites under the control clock scheme in which they can tunnel through to form the logic. The two polarizations of -1 and +1 represent the binary "0" and "1" respectively. The polarized charge can be transferred by the Coulombic repulsion within the square cells along with the one-dimensional cell array. There is nonlinear cell-to-cell interaction which means even when an input cell is slightly polarized, it can induced its polarization to the output cell to its extent which happens only when these cells are placed near one other and this was presented by P. Douglas Tougaw et. al [10]. The QCA wire [34-37] is a group of cells placed together to form a chain, as shown in figure 1(b). Neighboring cells along with others transmit binary information.

2 QCA MAJORITY IMPLEMENTATION

Binary basic elements also evolve with the development of logical devices such as parametrons and esaki diodes in 1960, as described by Yuhui Lu and Craig S. Lent [12]. The distributive law and algebraic manipulations in digital circuits with the use of majority logics[11-16]. The NOT gate is represented by rearranging the QCA cells as shown in figure 2(a). Inverter input is having "logic 0" and at the output we get "logic 1" or vice-versa. The majority gate shown in Figure 2 (b) has three inputs. A, B, and C act as input for three majority gate inputs, and the output is given by $M(A,$
B, C) = AB + BC + AC, expressing various logic gates by simply setting the inputs to zero or one.

(a)

Figure 2 (a) Inverter (b) Three input Majority gate

In figure 2(b) there is three input majority gate in which C has set at logic 0 and input A & B have set at logic 1, as a result AND gate is implemented by using majority gate functions, it will act as M(A, B, 0) = AB. On the other hand when we keep C input at logic 1, the majority gate functions become M(A,B,1) = (A + B) which act as an OR gate. The complex QCA circuit is designed using the five input majority gate which was described by Keivan Navia et. al [17] as shown in figure 3.
The majority structure uses the 10 QCA cells for the implementation where \( X_1, X_2, X_3, X_4, X_5 \) are the input logics of the five-input majority gate structure. The logic expression is represented by equation 2.

\[
M(X_1, X_2, X_3, X_4, X_5) = X_1X_2X_3 + X_1X_2X_4 + X_1X_3X_5 + X_1X_3X_4 + X_1X_4X_5 + X_2X_3X_4 + X_2X_3X_5 + X_2X_4X_5 + X_3X_4X_5
\]  

(2)

The clock signals in various digital circuits are main elements which synchronized the digital circuits and control the data flow. In the synchronization sequence, there are four different consecutive phases which are divided into four clock zones and the 90 degree out of phase, and four synchronization phases: "Switch", "Hold", "Release" and "Relax" [7-10]. As described in [4], the noise is much more concern in three input majority gate structure, thereby different clock zone are positioned at the input cells, middle QCA cells and output of the majority gate.
3 QCA BASED FLIP FLOP DESIGN

The flip flop circuit is the major component for the design of any memory device. The total number of QCA cells can be minimized by using majority logic in various designs of flip flops[19]. These flip flops are designed with optimum area in QCA designer and clocks cycles are utilized hence quantum area of these designs are studied. Here JK flip flop is discussed and simulated in QCA designer tool and power dissipation is estimated in QCA Pro tool.

3.1 QCA BASED JK FLIP FLOP DESIGN

The behavior of the JK flip flop is described in the characteristics table 1. The schematic of clocked JK flip-flop is shown in figure 5. The majority gate based flip flop is designed by using 2 inverters and four majority gates as shown in figure 6.
TABLE 1: CHARACTERISTIC TABLE OF JK FLIP FLOP

<table>
<thead>
<tr>
<th>CLOCK</th>
<th>J</th>
<th>K</th>
<th>Q(OUTPUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Q(PREVIOUS VALUE)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Q(TOGGLES)</td>
</tr>
</tbody>
</table>

\[ Q(output) = JQ' + K'Q \]  
(3)

The majority gate M1 is fed with complement of input K and Q which is feedback from output of the circuit. The Majority gate M2 act as OR gate to produced the output JQ’ + K’Q. The output of M1 and M3 are combined with the clock input by majority gate M2. The desired characteristics are produced in equation (3).

![Figure 6 Majority gate based JK Flip Flop](image6)

![Figure 7 QCA Cell Layout of JK Flip flop](image7)

The layout of JK Flip flop is implemented in QCA Designer shown in figure 7. The QCA implementation requires 39 cells to design, with an area of 0.04 \( \mu m^2 \) having 2 clock zones. The latency of the circuit is 0.5. The JK design utilizes 78% less area than...
previous design [34].

3.2 SIMULATION RESULT
The simulation result of JK flip flop as shown in figure 8, the output referred as Q having latency 0.5. The output is depicting the output as per the characteristic table 1. There is $90^0$ phase delay between the clocking zones. The JK flip flop having two clock zones so its vulnerability to noise is lesser then single QCA cell clock cycle.

Figure 8 Simulation result of QCA based JK Flip Flop

4 PERFORMANCE EVALUATION
The performance analyses of novel designed circuits are compared on the basis of their complexity, area, latency, and latency cost are given table 2. The quantum cost has been calculated on the basis of latency and area. It has been found that JK flip flop having complexity 39 cells and area utilization is 0.04 $\mu m^2$ than previous structure. The sequential circuits are designed using novel JK flip flop having 78% lesser complexity then previous structure. Further, in this paper 4 bit shift register is designed using QCA designer.
The layout of JK flip flop based shift register is shown in figure 9. The shift register is designed using proposed JK flip flop which was having 39 cells and the total area of 0.04 $\mu m^2$. The shift register serial in serial out is having the 4 JK flip flops, total QCA cell utilized are 238 cells with the area spacing of 0.20 $\mu m^2$. The input is feed through input D and clock is provided as shown in table 3 as the design vectors of shift-register and the simulation waveform in figure 10 is thus formed using these vectors using Euler Method in Coherence vectors Simulation Engine[27].

### TABLE 3 DESIGN VECTOR

<table>
<thead>
<tr>
<th>CLOCK</th>
<th>J</th>
<th>K</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
The 12800 are samples utilized with convergence tolerance of 0.001000, effective radius of cell is 65 nm and maximum iterations per sample is 100 in bistable simulations in the simulation engine of QCA designer tool[26].

Figure 9 Layout of the QCA based shift register

The Hamiltonian matrix is used to estimate the dissipation of energy and power in the QCA Cells array. Therefore, the energy dissipation of the QCA cell is one clock cycle of TCC = [-T, T], as described in equation 4.

\[
E_{diss} = \frac{\hbar}{2} \int_{-T}^{+T} \Gamma \, d\lambda \, dt = \frac{\hbar}{2} \left[ \int_{-T}^{+T} \Gamma \, d\lambda \right] + \left[ \int_{-T}^{+T} \lambda \, d\Gamma \right] \quad (4)
\]

The power dissipation model is given shown in equation 5. The table 4 shows the energy dissipation results.

\[
P_{diss} = \frac{E_{diss}}{T_{cc}} < \frac{\hbar}{2T_{cc}} \Gamma^2 + \left[ \int_{-T}^{+T} tanh\left( \frac{h\Gamma}{k_B T} \right) \right] = \frac{\Gamma^2}{|\Gamma^-|} tanh\left( \frac{h\Gamma^-}{k_B T} \right) \quad (5)
\]
6 CONCLUSION

In this paper, firstly an effective QCA based JK Flip Flop was re-design. The proposed structure consumes low energy and has a low complexity in comparison with the best reported design. The JK Flip Flop was designed and functionality, complexity is verified using QCA designer tool whereas the QCA pro was used for estimating energy dissipation. The results shows that the proposed JK flip flop utilizes 78% lesser complexity as compared to best reported structures. In the next step, by employing proposed JK flip flop, the 4 bit serial-in serial-out shift register has been constructed. The proposed 4-bit shift register using the JK flip-flop showed an improvement of 65% in terms of complexity and a 45% improvement in the occupation period of the region, respectively.

References


[26] QCA Designer Tool Version 2.0.3 http://www.mina.ubc.ca/qcadesigner_downloads


