Bidirectional Soft Switching Current fed LCL Resonant DC/DC Converter

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Abstract: This paper discusses non-isolated soft-switching bidirectional dc/dc converter for interfacing storage of energy in DC microgrid. The half bridge boost converter is applied at the input port. Subsequently, LCL resonant circuit is implemented to aid in soft switching of switches and diodes. A voltage gain of 2X is achieved using the voltage doubler circuit at the output. The overall voltage gain here is obtained from non-isolated circuit. The higher side voltage is halved by the capacitive divider to increase the step-down ratio. Low output voltage ripple is gained by the circuit by operating it at high frequencies. During buck/boost operation, Zero voltage turn on for switches and zero current turn on and turn off is achieved by diodes. Without the usage of external snubber circuit, the voltage stress across the semiconductor devices is clinched.

Keywords: bidirectional converter; DC Microgrid; buck-boost operation; zero voltage switching; zero current switching

1.INTRODUCTION

Depending upon non-renewable energy resources for producing electricity causes environmental pollution and hazardous to humans. As urban areas are developing at a faster rate, the generating plants are far from the residential areas due to huge population. Since they are situated farther from the residential areas a major amount of power is lost in the transmission itself. This creates the necessity for microgrid. When power generation is closer to the loads, the transmission losses are very negligible and efficiency is high. Here generation and distribution becomes comfortable therefore microgrid is being in emerging trends. The use of photovoltaic panels produces variable DC, regulated by means of the regulator or regulatory circuits and the fed to load.

DC micro grid architecture is shown in Fig.1. A 380V DC bus is used to transmit power to the load where several renewable energy sources and energy storage system generate power and feeds the bus. Usually DC energy storage devices rated with 48V whereas the DC bus is 380V. This demands for a buck-boost bidirectional converter for the cases of step up and step down the voltage as the ratio is almost 8 times. Hence the bidirectional buck/boost converter needs to operate in both the direction at extremely high duty ratio. This generally creates stress across the diodes, increasing the reverse recovery losses, resulting in low converter efficiency etc [3-6].

There are several isolated as well as non-isolated DC-DC converters that are in use currently. Non isolated converters usually have an edge over the others as some have low magnetic bulk, high efficiency and are very compact to use [7-9]. In order to achieve high power density high frequency switching of DC-DC converter is essential. Operating converter at high frequency exhibit very large switching losses, therefore soft switching was preferred. The bidirectional converters [10] reported earlier had high switching frequency of operation with high switching capability and high efficiency, but had limitations in step up/step down ratios [11-15]. The discussed [11] converter at high frequency but has a complicated inductor coupled design. In [12] the proposed topology is for wide load variation. In earlier paper, [16] converter of high efficiency and step up/step down ratio is used, but complications were reported in coupled inductor, hard switching limited frequency. The converter mentioned in paper [17] is not designed for soft switching purposes.

This paper shows a bidirectional DC-DC converter with soft switching LCL resonant having high step-up/step-down ratio. Fig.2. The merits of the projected model are as follows. 1) ZVS turn on of all switches during buck-boost operation. 2) ZVS turn on/turn off of all switches during buck-boost operation. 3) Voltage stress is low across the switches. 4) Voltage across the switches are clamped with adding any

![Fig. 1. Typical DC microgrid](url: http://www.ijpam.eu)
snubber circuit. 5) High frequency operation. 6) Decreased magnetic volume.

Fig. 2 The proposed converter

2. OPERATION OF CIRCUIT AND THE CONVERTER ANALYSIS

The converter discussed has boost converter (half bridge) followed by a LCL resonant circuit. This LCL combination increases the voltage gain of \( \frac{V_{in}}{1-d} \) and boosts up the voltage. The switches \( S_1 \) and \( S_2 \) are helpful in achieving ZVS and switches \( D_3 \) and \( D_4 \) are helpful in achieving ZCS. LCL combination is followed by voltage doubler which provides twice the gain in buck operation, the higher voltage is divided to half and further stepped down by the switches \( S_3 \) and \( S_4 \). LCL combination provides ZCS for diodes \( D_3 \) and \( D_4 \) and ZVS is provided by switches \( S_1 \) and \( S_2 \).

The gate pulses of the switches \( S_1 \) and \( S_2 \) are complementary to each other and switches \( S_1 \) and \( S_4 \) are off during boost operation. Similarly the gate pulses of the switches \( S_3 \) and \( S_4 \) are complementary to each other and switches \( S_3 \) and \( S_2 \) are off during buck operation.

A. Boost Operation

The switches \( S_1 \) and \( S_2 \) are on and \( S_1 \) and \( S_4 \) are off.

Interval-1 (Fig. 4a) \( (0 < t < t_1) \): Switches \( S_1 \) and \( S_2 \) are off. The difference between the inductor current and the resonant current starts discharging the parasitic capacitor \( C_{s1} \) and charges \( C_{s2} \). Power is transferred through the output capacitors \( C_1 \) and \( C_2 \). At \( t_1 \) the parasitic capacitor \( C_{s1} \) is discharged and \( C_{s2} \) is charged immediately. The current through the switches \( i_{s1} \) is \( 0 \), \( V_{s1} \) is \( 0 \), and \( V_{s2} \) is \( 0 \).

\[
\begin{align*}
V_{s2}(t_1) &= \frac{V_2}{T_0} \\
D &= \frac{T_0}{T_2} \quad T_0 &= \text{conduction of the main switch and } T_2 \text{ switching time period.}
\end{align*}
\]

Here the current flowing through the boost inductor \( i_L \) and the switch \( i_s \) are same i.e.i_s = i_L.

\[
\begin{align*}
V_{DQ2} &= L_2 \Delta i_L + C_2 \Delta V_{C2} \\
L_1 \Delta i_L + C_1 \Delta V_{C1} + C_{r2} \Delta V_{C_{r2}} &= 0
\end{align*}
\]

Where \( C_{r2} \) is the combination of all capacitors.

Interval-2 (Fig. 4b) \( (t_1 < t < t_2) \): At \( t=t_1 \) the parasitic capacitor \( C_{s1} \) gets discharged completely and \( C_{s2} \) gets charged completely. The difference between the inductor current and the resonant current discharges through anti parallel diode \( D_{s1} \) causing zero voltage across \( S_1 \). At \( t=t_2 \), \( D_{s1} \) is forward biased. \( L_1 \) and \( C_1 \) start to charge simultaneously \( C_1 \) and \( C_3 \) supply power to the load. Final values are

\[
\begin{align*}
i_{s2}(t_2) &= 0 \text{, } V_{s2}(t_2) = \frac{V_{low}}{1-D}, \text{ } V_{s1}(t_2) = 0 \\
i_{D_{s1}}(t_2) &= i_{s2}(t_2) - i_{s1}(t_2) \\
V_{C2} - V_{low} - L_1 A_{in} + D_2 R_s (i_{s1} - i_{s2}) - V_{C1} &= 0
\end{align*}
\]

Interval-3 (Fig. 4c) \( (t_2 < t < t_3) \): At \( t=t_2 \) switch \( S_1 \) is turned on using ZVS. \( L_B \) starts decreasing. The current through the resonant inductor \( L_B \) decreases linearly through the switch \( S_1 \), capacitor \( C_{s3} \), resonant inductor \( L_B \) and resonant capacitor \( C_{r3} \). The diode \( D_{s3} \) still conducts to charge \( C_2 \) and \( D_{s3} \) is reversed biased. Power reached the load through \( C_{r3} \)

\[
\begin{align*}
i_{s3}(t) &= i_{s2}(t) - i_{s1}(t) \\
V_{low} - L_B A_{in} &= V_{C1} - V_{C2} - \alpha
\end{align*}
\]
Fig. 4. Equivalent circuits of the converter operation in boost mode.

**Interval-4** (Fig. 4d) \((t_2 < t < t_3)\): At this interval \(S_1\) is still in on state. The anti-parallel diodes at the output side are reverse biased. Load receives the power from the output capacitor \(C_3\) and \(C_5\). At \(t=t_3\), switch \(S_1\) is turned off. Here \(V_{DS3}=0\), \(V_{S4}=0\), \(V_{S2}=\frac{V_{High}}{1-D}\)

Here \(i_{S1}=i_{LB}\)

\[i_{LB}(t) = i_{LB}(t_3) - \frac{(V_{CL1} - V_{CL2} - V_{DS3})}{L_2} \]  

\[i_{LB}(t_3) = \frac{V_{CL1} - V_{DS3}}{L_1} \]  

\[\text{Interval-5} \quad (t_3 < t < t_4): \] Switches \(S_1\) and \(S_2\) are off. Parasitic capacitor \(C_{S1}\) gets charged completely meanwhile \(C_{S2}\) gets discharged. No power reached the load from input end to output end because no diodes are conducting at the output side. So load is powered by \(C_3\) and \(C_4\). At this time \(C_{S2}\) gets discharged and \(C_{S1}\) gets charged to \(\frac{V_{High}}{1-D}\).

\[V_{High} = V_{High/2} + V_{High/2} \]  

\[V_{CL1} - L_{2} \frac{di}{dt} - D_{S3} R i_{LB} - V_{High/2} = 0 \]  

**Interval-6** (Fig. 4f) \((t_4 < t < t_5)\): Anti parallel diode \(D_{S3}\) starts conducting by differences of \(i_{LB}\) and \(i_{LB}\) where \(S_1\) is provided with gating pulse for ZVS turn-on. Antiparallel diodes in the output side are all reverse biased. Therefore \(i_{S3}(t_6) = 0\), \(i_{S3}(t_5) = 0\), \(V_{S3} = \frac{V_{Low}}{1-D}\).

\[i_{S3}(t_6) = i_{S3}(t_5) = 0 \]  

\[i_{D_{S3}}(t_6) = i_{D_{S3}}(t_5) - i_{S3}(t_5) \]  

\[V_{Low} = L_{2} \frac{di}{dt} + D_{S3} R (i_{S3} - i_{LB}) = 0 \]  

**Interval-7** (Fig. 4g) \((t_5 < t < t_6)\): At \(t=t_4\) switch \(S_2\) is turned on using ZVS. \(L_{1}\) starts charging. Inductor \(L_{1}\), capacitors \(C_{r}\) and \(C_{S4}\) are resonance with each other. The diode \(D_{S3}\) is
forward biased and conducts throughout this interval. At \( t=t_7 \), diode \( D_3 \) turns off.

\[
\begin{align*}
\dot{i}_{L_2}(t) &= \dot{i}_{L_2}(t_6) + \frac{V_{H_2}}{L_2} (t - t_6) \\
i_{L_2} &= (V_{C_2}(t_6) + V_{C_3}(t_6))
\end{align*}
\]

Interval 8 (Fig. 4b) \( t_7 < t < t_8 \): All diodes in output side, turns off and power is transferred by to load by the capacitor \( C_4 \). Switch \( S_3 \) is ON and inductor \( L_4 \) stores energy in it. At \( t=t_7 \) \( S_2 \) is turned OFF.

### B. Buck Mode Operation:

The operating waveforms of the converter in buck mode are as shown in Fig. 5. \( S_1 \) and \( S_2 \) are switched off during the whole buck operation.

#### Interval 1 (Fig. 6(a); \( t_0 < t < t_1 \)): In the beginning of this interval, switches \( S_3 \) and \( S_4 \) are turned off. Parasitic capacitor \( C_{S2} \) starts discharging and capacitor \( C_{S4} \) starts charging via resonant current \( i_{L_2} \). Through the output capacitor \( C_4 \), the power is transferred to load. Resonant inductor \( L_1 \) current \( i_{L_1} \) path is completed from \( D_{S2} \). At the end, the parasitic capacitor \( C_{S4} \) is completely charged to \( V_{H04} \) and \( C_{S2} \) is fully discharged. The final values of components are \( i_{S3}(t_1) = 0 \), \( i_{S3}(t_1) = 0 \), \( V_{S3}=V_{H04} \) and \( V_{S4}=0 \). Resonant inductor \( L_1 \) current is

\[
i_{L_1}(t)=\frac{V_{S1}}{Z_1} = \frac{V_{S1}}{Z_1}
\]

#### Interval 2 (Fig. 6(b); \( t_1 < t < t_2 \)): In the beginning of this interval, \( C_{S2} \) is fully discharged and parasitic capacitor \( C_{S3} \) is charged to maximum. Resonant inductor \( L_2 \) current \( i_{L_2} \) flows via anti parallel diode \( D_{S3} \) resulting in zero voltage condition across switch \( S_3 \). There is still conduction in Diode \( D_{S2} \) and diode \( D_{S1} \) is under reverse bias. The final values are \( i_{S3}(t_2)=0 \), \( i_{S4}(t_2)=0 \), \( V_{S3}(t_2)=0 \) and \( V_{S4}(t_2)=V_{H04} \). Resonant inductor current \( L_2 \) is given by

\[
\Delta i_{L_2} = \frac{V_{S1} + 5V_{H04}}{z_2}
\]

Interval 3 (Fig. 6(c); \( t_2 < t < t_3 \)): When \( t=t_2 \), switch \( S_3 \) is ZVS switched on. A voltage \( V_{H03} \) is applied on resonant circuit via switch \( S_3 \). Resonant inductor \( L_3 \) and capacitor \( C_r \) resonate with capacitor \( C_4 \). Through output capacitor \( C_0 \), the output side energy is transferred to load. The freewheeling energy stored in inductor \( L_8 \) is conducted through diode \( D_{S3} \). The current through resonant inductor \( L_2 \) i_{L_2} continues to flow through diode \( D_{S2} \). This interval ends at \( t=t_3 \) when switch \( S_3 \) is turned off.

Interval 4 (Fig. 6(d); \( t_3 < t < t_4 \)): Switches \( S_3 \) and \( S_4 \) in this interval are turned off. Parasitic capacitor \( C_3 \) starts discharging and capacitor \( C_j \) starts charging through resonant current \( i_{L_2} \). Antiparallel diode \( D_3 \) still operates in forward bias. Power supply to load is still by output capacitance \( C_0 \). When \( t=t_4 \), parasitic capacitance \( C_4 \) is fully discharged while parasitic
capacitance $C_3$ is fully charged to $V_H$. The final values of these parameters are $i_{S3}(t4) = 0$, $i_{S4}(t4) = 0$, $V_{S3}(t5) = V_H$, $V_{S4}(t5) = 0$.

Fig. 6. Equivalent circuits of the converter in buck mode

Interval 5 (Fig. 6(e); $t4 < t < t5$): During this interval, the antiparallel diode $D4$ starts to conduct through resonant inductor current $i_{Lr2}$ so that $S4$ could be gated for turn on by ZVS. The antiparallel diode $D2$ is still conducting along the output side. By this interval end the antiparallel diode $D2$ turns off by ZCS. The final values of these parameters $i_{S3}(t5) = 0$, $i_{S4}(t5) = 0$, $V_{S4}(t5) = 0$, $V_{S3}(t5) = V_H$.

Interval 6 (Fig. 6(f); $t5 < t < t6$): At $t = t5$ with zero voltage across it, switch $S_4$ is turned on. Switch $S_4$ diverts the resonant current $i_{Lr2}$. Antiparallel diode $D1$ is forward at start of this interval and capacitor $C_5$ starts charging. At $t = t6$ antiparallel diode $D1$ turns off with zero current.

Interval 7 (Fig. 6(h); $t6 < t < t7$): neither of the anti-parallel diode $D1$ and $D2$ is conducting. For this complete interval, switch $S4$ is turned on. At $t = t7$ switch $S4$ goes off.

III. VOLTAGE RATIO IN DIFFERENT MODES

A. Boost mode gain

The overall gain of the converter is contributed by its three stages. The gain given by front end of the half bridge boost converter is $V_L/(1-D)$. This is followed by LCL resonant circuit which provides a voltage gain corresponding to the switching frequency. The final part of the circuit which is the voltage doubler, further improves converter gain by 2x. The overall gain is given by

$$V_{boost} = \frac{V_{in} \cdot G_{boost}(f) \cdot 2}{1 - D}$$  \hspace{1cm} (27)

Where $G_{boost}(f) = \frac{X_{L1} + X_{L1} + R_{ac}}{X_{L1} + X_{L1} + R_{ac}} + R_{ac}$

$D_{boost} =$ duty cycle, $f$ is switching frequency, $R_{ac}$ is effective resistance of AC load which is $R_{ac} = 2R_{ac}$, $X_C, X_{L1}, X_{L2}, X_{L2}, X_{L2}$ are reactance of $C_1, L_1, L_2$ respectively.

Fig.10(d) shows the output power variations and its effects on gain. Load power is directionally proportional to the gain. It can be observed that the gain of the proposed converter is influenced by frequency, as frequency enhances gain increases.

B. Buck mode ratio:
Only half the voltage \( V_{l} \) is applied to the resonant component on account of voltage divider circuit. The overall step down ratio can be expressed as

\[
V_{Low} = 0.5V_{High}D_{Back}G_{Back}(f)
\]  

Where \( G_{Back}(f) = \frac{x_{L1}C_{L1}^{2} + x_{L2}C_{L2}^{2}}{x_{L1}^{2}C_{L1}^{2} + x_{L2}^{2}C_{L2}^{2}} \)

Fig. 8(a) illustrates the gain \( G \) dependency of load. The buck ratio for higher load is much less as compared to that at a lower load. Fig. 8(b) illustrates the relation between overall ratios in buck mode when switching frequency is varied. It can be seen that step down ratio is dependent on switching frequency as frequency goes up, step down ratio increases.

IV. DESIGN OF THE CONVERTER

The design methodology for the converter by means of an example for the following specifications is discussed here: \( V_{Low}=48V \), \( V_{High}=380V \), output power, \( P_{O}=350W \). The following are the assumptions made:

(a) Converter efficiency is presumed as 100%.

(b) Voltage ripples across capacitor \( C5, C6, C7 \) and \( C8 \) to be very insignificant or minute.

(c) All the components are ideal and lossless. To decide the current ratings, the design equations are derived:

1) Average current through input inductor is given by

\[
I_{L1} = \frac{V_{L}}{\pi f_{L1}} = 6.25A
\]  

(29)

2) At input voltage duty ratio is selected, i.e., \( V_{L} = 48V \) and full load based on maximum switch voltage rating.

\[
D_{Boost} = \frac{V_{High} - V_{Low}}{V_{High}}\sqrt{\frac{f_{L1}}{f_{L2}}} = 0.699
\]  

(30)

3) Value of input boost inductor is given by

\[
L_{2} = \frac{V_{High}}{f_{L2}D_{Boost}}
\]  

(31)

Where, \( \Delta I_{L1} \) is the boost inductor ripple current. For,

\[
\Delta I_{L1}=2A, L_{1}=159.77\mu{H}
\]

4) Sufficient energy difference stored in inductor \( L_{1} \) and \( L_{2} \) is supposed to be maintained to achieve ZVS of lower switch \( S_{2} \) and the capacitance \( C_{3} \) and discharge \( C_{2} \) is given by

\[
\frac{1}{2} L_{1}E_{mg}^{2} - \frac{1}{2} L_{2}E_{mg}^{2} > \frac{1}{2} (C_{31} + C_{32})(\frac{V_{g}^{2}}{1-f_{L2}})
\]  

(32)

To ensure ZVS turn on of switch \( S_{1} \) the energy stored in resonant inductor \( L_{2} \) at \( t=t_{1} \) has to be greater than energy stored in device capacitances of \( S_{1} \) and \( S_{2} \) and is given by

\[
\frac{1}{2} L_{2}E_{mg}^{2}(t_{2}) > \frac{1}{2} (C_{S1} + C_{S2})(\frac{V_{g}^{2}}{1-f_{L2}})
\]  

(33)

### Table 1 Converter Specifications

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low side voltage ( V_{low} )</td>
<td>48V</td>
</tr>
<tr>
<td>High side voltage ( V_{high} )</td>
<td>380V</td>
</tr>
<tr>
<td>Rated power ( P_{O} )</td>
<td>350W</td>
</tr>
</tbody>
</table>

In order to ensure ZVS for switch \( S_{b} \), the energy stored in resonant inductor \( L_{2} \) at \( t=t_{1} \) has to be greater than energy stored in device capacitances of \( S_{1} \) and \( S_{2} \) and is given by

\[
\frac{1}{2} L_{2}E_{mg}^{2}(t_{1}) > (C_{S1} + C_{S2})(\frac{V_{g}^{2}}{1-f_{L2}})
\]  

(34)

Similarly, for \( S_{a} \) ZVS condition is energy stored in resonant inductor \( L_{2} \) at \( t=t_{4} \) has to be greater than energy stored in device capacitance of switch \( S_{1} \) and \( S_{2} \) and is given by

\[
\frac{1}{2} L_{2}E_{mg}^{2}(t_{4}) > (C_{S1} + C_{S2})(\frac{V_{g}^{2}}{1-f_{L2}})
\]  

The resonant frequency of the LCL is given by

\[
\nu_{r} = \frac{1}{\sqrt{\frac{C_{1}C_{2}}{C_{1}+C_{2}}}}
\]  

(36)

For resonant frequency of 91.93 kHz the \( C_{1}=C_{2}=100\mu{F}, L_{1}=L_{2}=30\mu{H} \) and \( C_{1}=0.1\mu{F} \).

V. PROTOTYPE RESULTS

The designed converter rated at 350W was simulated to test verify the steady-state operation, analysis and design of the proposed converter. Table I shows the specifications. For both buck and boost operation, it was tested with \( V_{low} = 48V \) and \( V_{high} = 380V \) at full load (350W). Experimental results for boost operation are shown in Fig. 7. Fig. 7(b) confirms the ZVS turn on of switch \( S_{1} \) since anti-parallel diode \( D_{51} \) is conducting causing zero voltage across \( S_{1} \) before gating signal is applied. In waveforms shown in Fig. 7(d) the input and output current reads 0.7A and 8.4A. In Fig. 7(c) it can be seen that antiparallel diode \( D_{3} \) and \( D_{4} \) conduct and commutate with zero current. Therefore, reverse recovery losses are not present. Fig. 7(e) shows that input voltage 48V is stepped-up to 380V with small voltage ripple in the output voltage; boost inductor ripple current is also small.

**Boost operation:**
Fig 7: (a) Current through L1 & L2, Voltage across Cr (b) ZVS turn on of S1 (c) Current and Voltage across D2, D3 (d) Output and input current waveforms (e) Step up voltage from 48V and 380V

Buck operation:

Fig 8: (a) Current and voltage through D2 (b) Current through L, L1, L2 (c) ZVS turn-ON of switch S3 (d) ZVS turn-ON of switch S4 (e) Voltage and Current of S3.

The experimental results for buck operation are shown in Fig. 8. Fig. 8(c) shows the gating signals for switch S3, it can be seen that antiparallel diode conducts before the gating signal is applied causing ZVS turn-on of the switch S3. Similarly, ZVS turn-on of switch S4 is observed in Fig. 8(d). In Fig. 8(a) anti-parallel diode D2 commutates with zero current. Therefore, reverse recovery losses are insignificant in this case. It can be observed that the experimental waveforms coincide with analytically predicted steady-state operating waveforms. The converter maintains soft-switching under varying load conditions.

VI. CONCLUSIONS

In this paper, transformer-less LCL resonant soft-switching bidirectional dc/dc converter is proposed. High step up/step down ratio, high efficiency, low device voltage stress, ZVS turn-on for all switches and ZCS turn-on and turn-off for all
diodes in both buck/boost mode of operation were the key features of this prototype. For the wide load range, the suggested converter can achieve ZVS for switches and ZCS for diodes. Without the external snubber circuit, the device voltage is maintained. Simulation results have been manifested to verify the suggested analysis, design and soft-switching, and to validate the performance of the converter. The converter maintains high efficiency for both the direction of power flow.

REFERENCES
