Non-isolated High gain DC-DC converter by Quadratic boost converter and voltage Multiplier cell

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Abstract

A novel non- isolated DC-DC converter is proposed by combining quadratic boost converter with voltage multiplier cell. The proposed converter has low semiconductor devices voltage stress and switch utilization factor is high. The superiority of the converter is voltage stress of the semiconductor devices depends on voltage multiplier (VM) cell. By increasing the VM cell the stresses across the devices reduces drastically. The Proposed converter has same number of components compared to certain voltage lift converters taken for comparison. A detailed comparative study is made on the proposed converter with few voltage lift converters in literature, conventional boost with VM cell and quadratic boost converter. A 40W prototype is constructed with 12V input voltage and 96V output voltage to verify the performance and validate the theoretical analysis of the proposed converter.

Key Words : High gain; Quadratic;Multiplier;CCM; DCM;Voltage stress;Efficiency.
1 Introduction

High gain dc-dc converter topologies are derived for MEA (More Electric Aircraft), Micro and Nano satellite Electric Thrusters during last decades. Introduction of electric propulsion system need a dedicated dc-dc converter to convert the solar energy for electric thruster [1-3]. Electric thruster requires a high DC voltage of around tens of kV depending on the type of electric thruster used [4]. Recent trend in power distribution in MEA is the use of high voltage DC system. Certain values of system voltage under research are 270, 350 and 540V [5]. Bidirectional DAB (Dual Active Bridge) dc-dc converter is introduced in [6] to meet the power demands of aircraft electric loads. Boosting type converters are required boosting low level voltage from PV to the desired level of voltage. Using conventional boost converter, voltage step up can be obtained by increasing the duty cycle nearer to unity. By increasing the duty cycle the conduction loss, switching loss are increased which results in low efficiency [7][8]. Series connection of multiple boost converter results in high voltage gain. However, cost of the converter is increased due to too many components [9]. By escalating the turns ratio of the transformer in isolated DC-DC converter, large voltage conversion ratio can be obtained. However the diode stress voltage and voltage spikes across the switches should be considered with certain remedial measures [10-13][30]. Large voltage gain can be achieved with coupled inductor in the converters [14][16]. However, they suffer with similar disadvantages of isolated DC-DC converters. By incorporating switched capacitor or switched inductor in the converter the voltage conversion ratio can be increased. Moreover, voltage regulation is poor [17]. Based on 3SSC (three state switching cell) high voltage gain converter is introduced. However, the circuit weight and volume is high due to the presence of autotransformer. Soft switching techniques are incorporated in high step up topologies to improve its performance [31].
2 High voltage gain converters with voltage multiplier cell

The notable application of voltage multiplier cells are Travelling wave tube amplifier and capacitor charge transference [18][19]. In both the applications, it step ups the voltage to very high level without the use of magnetic components. Incorporation of voltage multiplier to DC-DC converter is not new and many articles were published in literature. High voltage gain converter is introduced with capacitor voltage stacking cell [20]. However, the current stress results in the circuit. Four switch high gain converter is introduced by employing cockroft- walton voltage multiplier cell [21]. The conducting state of the switches are very complicated in that topology. The advantages of Voltage multiplier based step up converters are follows:

- Diode-capacitor multiplier (VM cell) can be added to the topology without modifying the original topology.
- No additional switch is needed apart from the main switch of the circuit which simplifies the gate drive circuit.
- Main switch, multiplier and output diode voltage stress depends on the number of multiplier cell. As a result of this switch with low on-state resistance can be used that minimize the losses and improves the converters efficiency.

Table 1 gives the comparison of different topology with voltage multiplier. Several topologies are derived by integrating voltage multiplier with voltage lift or coupled inductor or 3SSC or D-C-L unit. It is found from the comparison that there is no promising topology which satisfies both voltage gain and voltage stress across the switch with less number of components. The proposed converter operating principle is given in section 3. Steady state (DC) analysis is made in section 4. Section 5 describes about the component design and power losses of the converter. A comparative study is made in the section 6. Section 7 presents the simulated and hardware results of the proposed converter.
Table 1 Comparison of different topology with voltage multiplier in literature

<table>
<thead>
<tr>
<th>Ref</th>
<th>Technique</th>
<th>Voltage gain</th>
<th>Voltage across switch</th>
<th>No of component</th>
</tr>
</thead>
<tbody>
<tr>
<td>[22]</td>
<td>N units of D-C-L, n number of voltage multiplier cell</td>
<td>( \frac{3n + 4D + 2}{1 - D} )</td>
<td>( \frac{3n + 4D + 2}{n - 2} )</td>
<td>( (n+2) )</td>
</tr>
<tr>
<td>[23]</td>
<td>N units of D-C-L, Voltage multiplier cell</td>
<td>( \frac{5 + D}{1 - D} )</td>
<td>( \frac{S}{n + 2} )</td>
<td>( (n+2) )</td>
</tr>
<tr>
<td>[24]</td>
<td>Modified interleaved Boost converter with Voltage multiplier</td>
<td>( \frac{1 - D}{2N + 1} )</td>
<td>( \frac{2(N + 1)}{n - 2} )</td>
<td>12</td>
</tr>
<tr>
<td>[25]</td>
<td>Interleaved Boost converter with Voltage multiplier</td>
<td>( \frac{1 - D}{N + 1} )</td>
<td>( \frac{N + 1}{n - 1} )</td>
<td>11</td>
</tr>
<tr>
<td>[26]</td>
<td>Three winding high-frequency coupled inductor and voltage multiplier</td>
<td>( \frac{1 - D}{N + 1} )</td>
<td>( \frac{N + 1}{2(N + 1)} )</td>
<td>15</td>
</tr>
<tr>
<td>[27]</td>
<td>Three stage switching cell and voltage multiplier</td>
<td>( \frac{1 - D}{N + 1} )</td>
<td>( \frac{n + 1}{n - 1} )</td>
<td>15</td>
</tr>
<tr>
<td>[28]</td>
<td>Coupled inductor and voltage multiplier</td>
<td>( \frac{1 - D}{N + 1} )</td>
<td>( \frac{N + 1}{n - 1} )</td>
<td>17</td>
</tr>
<tr>
<td>[29]</td>
<td>Voltage lift Voltage multiplier clamp mode and coupled inductor</td>
<td>( \frac{1 - D}{N + 1} )</td>
<td>( \frac{n + 1}{n - 1} )</td>
<td>17</td>
</tr>
</tbody>
</table>

3 Operating principle of the proposed converter in CCM mode

Fig.1 illustrates the topology of the proposed converter, which consists of main switch SW, two inductors \((L_1, L_2)\), Diode \((D_1, D_2)\) and a Voltage multiplier cell consist of two capacitance \((C_{M1}, C_{M2})\), two diode \((D_{M1}, D_{M2})\) and one resonance inductor \(L_r\). There are five main modes during one switching cycle. The Modes of operation with current flow path are shown in Fig 2. Fig 3 demonstrates some typical waveforms obtained during continuous conduction mode (CCM).

![Figure 1: Proposed converter](image-url)
Figure 2: Equivalent circuit representing five operating modes with current flow path in CCM operation. (a) Mode I. (b) Mode II. (c) Mode III (d) Mode IV (e) Mode V

Mode I \([0, t_0]\): The switch SW is conducting at this mode. The input inductor \(L_1\) is charged by the input DC source \(V_g\) and the inductor \(L_2\) is charged in parallel by the capacitor \(C_1\). The capacitor \(C_{M1}\) and \(C_{M2}\) are charged to the output voltage of the quadratic boost converter with VM cell \((V_gM/[1D]^2)\) through the diode \(D_{M2}\). The average voltage of \(C_{M1}\) and \(C_{M2}\) are equal.

Mode II \([t_0, t_1]\): During this mode the switch SW is on state. At this instant \((t_0)\) diode \(D_{M2}\) turns off. The input inductor \(L_1\) is charged by the input DC source \(V_g\) and the inductor \(L_2\) is charged in parallel by the capacitor \(C_1\). It is similar to Quadratic boost converter with switch in conducting state. The inductors \(L_1, L_2\) stores energy until the switch SW turns off at the instant \((t_1)\).

Mode III, V, VII \([t_1, t_2]\): At this instant \((t_1)\), switch SW turns off. Diode \(D_2, D_{M1}\) and \(D_0\) turns on and the energy accumulated in the inductors \(L_1, L_2\) are transmitted to the output capacitor \(C_0\) through the diode \(D_0\). It is also transmitted to the capacitor \(C_{M2}\) through the diode \(D_{M1}\) and to the capacitor \(C_1\) through the diode \(D_2\). This mode is just similar mode 5 and 7.

Mode IV \([t_2, t_3]\): During this mode the switch SW is off state. At this instant \((t_2)\) diode \(D_{M1}\) turns off. The energy accumulated
in the inductors $L_1, L_2$ is transmitted to the output capacitor $C_0$ through the diode $D_0$. At the end of this mode ($t_3$) diode $D_{M1}$ turns on again and enters into the mode similar to mode 3.

Mode IV [$t_4$, $t_5$]: At this instant ($t_4$) diode $D_0$ turns off. The energy accumulated in the inductors $L_1, L_2$ is transmitted to the output capacitor $C_{M2}$ through the diode $D_{M1}$. At the end of this mode ($t_5$) diode $D_0$ turns on again and enters into the mode similar to mode 3.

Figure 3: Current waveforms of the proposed converter
4 Steady state performance analysis of proposed converter

To simplify the analysis only stages 1 and 3 are considered for CCM operation because the time durations of mode 4 and 6 are short. Mode 3, 5 and 7 are similar. At mode 1, the main switch SW is in ON condition, the inductor $L_1$ is charged by the input dc source $V_g$, and the inductors in the switched inductor cells are charged by the voltage across $C_1$. The following equations are obtained from fig 2(a)

\[ V_{L1} = V_g \] (1)
\[ V_{L2} = V_{C1} \] (2)

During mode 3, the main switch SW is turned OFF, the inductors $L_1$, $L_2$ are discharged. The voltages across the inductor $L_1$ and $L_{S1}$, $L_{S2}$ can be

\[ V_{L1} = V_g - V_{C1} \] (3)
\[ V_{L2} = V_{C1} - V_{CM1} \] (4)

During the mode 1 Capacitor $C_{M2}$ is charged with the output voltage of quadratic boost converter with voltage multiplier cell. After mode 4, the load voltage is equal to two times of capacitor voltage $C_{M2}$ for one multiplier cell $[M=1]$ similar to the converter in [19].

\[ V_O = 2V_{CM2}......M = 1 \] (5)

Administering a volt-second balance on the inductor $L_1$, $L_2$ produces

\[ \int_0^{DT_s} V_g dt + \int_{DT_s}^{T_s} (V_g - V_{C1}) dt \] (6)
\[ \int_0^{DT_s} V_{C1} dt + \int_{DT_s}^{T_s} (V_{C1} - V_{CM1}) dt \] (7)
Solving equation (6) yields

\[ V_{C1} = \frac{V_g}{1 - D} \]  

(8)

By substituting (8) in to (7) respectively, \( V_{CM2} \) and \( V_O \) can be obtained as

\[ V_{CM1} = \frac{V_g}{(1 - D)^2} \]  

(9)

\[ G_{V-CCM} = \frac{V_O}{V_g} = \frac{[m+1]}{[1-D]^2} \]  

(10)

Table 2 Component stresses and average values of introduced converter

<table>
<thead>
<tr>
<th>Proposed converter</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage stress of the diodes in voltage multiplier cell</td>
<td>( D_{M1} )</td>
</tr>
<tr>
<td></td>
<td>( D_{M2} )</td>
</tr>
<tr>
<td>Voltage stress of the diodes in QB</td>
<td>( D_1 )</td>
</tr>
<tr>
<td></td>
<td>( D_2 )</td>
</tr>
<tr>
<td>Voltage stress of the switch</td>
<td>SW</td>
</tr>
<tr>
<td>Average voltage of the switch</td>
<td>SW</td>
</tr>
<tr>
<td>Average voltage of the diodes in voltage multiplier cell</td>
<td>( D_{M1} )</td>
</tr>
<tr>
<td></td>
<td>( D_{M2} )</td>
</tr>
<tr>
<td>Average voltage of the diodes in QB</td>
<td>( D_1 )</td>
</tr>
<tr>
<td></td>
<td>( D_2 )</td>
</tr>
<tr>
<td>Average current of the diodes in QB</td>
<td>( D_1 )</td>
</tr>
<tr>
<td></td>
<td>( D_2 )</td>
</tr>
<tr>
<td>Average Inductor current</td>
<td>( L_1 )</td>
</tr>
<tr>
<td></td>
<td>( L_2 )</td>
</tr>
<tr>
<td>Average current of the diodes in voltage multiplier cell</td>
<td>( D_{M1} )</td>
</tr>
<tr>
<td></td>
<td>( D_{M2} )</td>
</tr>
<tr>
<td>Average current of the switch</td>
<td>SW</td>
</tr>
<tr>
<td></td>
<td>( [1 - D]^3 )</td>
</tr>
<tr>
<td>Average capacitor current</td>
<td>( C_1 )</td>
</tr>
<tr>
<td></td>
<td>( [1 - D]^2 )</td>
</tr>
</tbody>
</table>
5 Design and paper analysis of proposed converter

Based on the analytical expression of the operation of converter, the design values of the components are selected.

5.1 Design of inductor $L_1$ and $L_2$

In case of switch ON condition, inductor current $i_{L1}$ and $i_{L2}$ peak to peak ripple relation is obtained as follows,

$$\Delta i_{L1} = i_{L1}(DT) = \frac{V_g DT}{L_1}$$  \hspace{1cm} (11)

$$\Delta i_{L2} = i_{L2}(DT) = \frac{V_{C1} DT}{L_2} = \frac{V_g D/1-D}{L_2 f_s}$$  \hspace{1cm} (12)

At the boundary condition,

$$I_{OB} = \frac{\Delta i_{L1}}{2}$$  \hspace{1cm} (13)

$$L_{1min} = \frac{|1-D_{min}|^2 R_{Lmax}}{2(1+D_{min}) f_s}$$  \hspace{1cm} (14)

$$L_{2min} = \frac{|1-D_{min}|D_{min} R_{Lmax}}{2f_s}$$  \hspace{1cm} (15)

From (14) and (15) $L_1$ and $L_2$ are selected as 0.119mH and 0.239mH respectively.

Resonant inductor limits the current variation and minimizes the commutation losses. It depends on $di/dt$ (maximum current variation) at turn on time. The value of resonant inductor is selected as 0.5uH

5.2 Design of capacitor

The input and output capacitors minimum value depends on output voltage, load resistance and the operating frequency.

$$C_{min} = \frac{V_o D_{max}}{R_{Lmin} f_s}$$  \hspace{1cm} (16)

From (16) input and output capacitor are selected as 22uF. The voltage multiplier capacitors minimum value depends on maximum...
power, multiplier capacitor voltage and operating frequency.

\[ C_{M1\min} = \frac{P_{\text{max}}}{V_{\text{CM}}^2 f_s} \]  

(17)

From (17) voltage multiplier capacitor is selected as 0.5\( \mu \)F

**5.3 Power loss analysis**

Table 2 gives the average and maximum voltage of the semiconductor devices and other components in the proposed converter.

RMS Current through the switch SW is

\[ i_{SW\text{rms}} = \sqrt{\frac{1}{T} \int_0^{DT} [i_{L1} + i_{L2}]^2 \, dt} \]  

(18)

Hence, ohmic power loss in switch is

\[ P_{SW} = i_{SW}^2 R_{DS} = \frac{i_o^2 [2-D]^2 D}{[1-D]^2} r_{DS} \]  

(19)

The RMS current through the diode can be given as

\[ i_{D1\text{rms}} = \sqrt{\frac{1}{T} \int_0^{DT} i_{L1}^2 \, dt} = \frac{i_o \sqrt{D}}{\sqrt{1-D}} \]  

(20)

\[ i_{D2\text{rms}} = \sqrt{\frac{1}{T} \int_0^{DT} i_{L2}^2 \, dt} = \frac{i_o \sqrt{1-D}}{\sqrt{D}} \]  

(21)

\[ i_{DM1\text{rms}} = \sqrt{\frac{1}{T} \int_0^{DT} [i_{L1} - i_{L2}]^2 \, dt} = \frac{i_o D \sqrt{1-D}}{\sqrt{1-D}} \]  

(22)

\[ i_{DM2\text{rms}} = \sqrt{\frac{1}{T} \int_0^{DT} i_{L2}^2 \, dt} = \frac{i_o \sqrt{D}}{\sqrt{1-D}} \]  

(23)

\[ i_{D0\text{rms}} = \sqrt{\frac{1}{T} \int_0^{DT} i_{L1}^2 \, dt} = \frac{i_o \sqrt{D}}{\sqrt{1-D}} \]  

(24)

The power loss in forward resistance \( R_F \) of the diode is given as

\[ P_{RF} = [i_{D1\text{rms}}^2 + i_{D2\text{rms}}^2 + i_{DM1\text{rms}}^2 + i_{DM2\text{rms}}^2 + i_{D0\text{rms}}^2] R_F \]  

(25)

The average current through the diode can be given by

\[ i_{D1\text{avg}} = \frac{1}{T} \int_0^{DT} i_{L1} \, dt = \frac{i_o D}{\sqrt{1-D}} \]  

(26)
The power loss due forward voltage drop in diode is given by

\[ P_{VF} = V_F \left[ i_{D1avg} + i_{D2avg} + i_{DM1avg} + i_{DM2avg} + i_{D0avg} \right] \quad (30) \]

From (25), (30) total power loss in diode is obtained as

\[ P_D = P_{RF} + P_{VF} \quad (31) \]

RMS value of the inductor current can be derived as

\[ i_{L1rms} = \frac{i_0}{\sqrt{1-D}}, \quad i_{L2rms} = \frac{i_0}{\sqrt{1-D}}, \quad i_{Lrrms} = \frac{i_0}{\sqrt{1-D}} \quad (32) \]

Power loss associated with inductor can be derived using (32)

\[ P_L = i_{L1rms}^2 r_{L1} + i_{L2rms}^2 r_{L2} + i_{Lrrms}^2 r_{Lr} \quad (33) \]

Capacitor current RMS values can be given by

\[ i_{C1rms} = \frac{i_0 D}{\sqrt{1-D}}, \quad i_{CM1rms} = \frac{i_0 (1-2D)}{\sqrt{1-D}} \quad (34) \]

Capacitor power losses can be derived from (34)

\[ P_C = i_{C1rms}^2 r_{C1} + i_{CM1rms}^2 r_{CM1} \quad (35) \]

Total power loss in the converter is

\[ P_{LOSS} = P_{SW} + P_D + P_L + P_C \quad (36) \]

The efficiency of the proposed high step up converter is given by
Efficiency = \eta = \frac{P_0}{P_{in}} = \frac{1}{1 + (P_{LOSS}/P_0)} \tag{37}

6 Comparison of proposed converter with other high voltage gain converter

Two different comparisons were done in order to highlight the advantage of the proposed converter. The four converters taken for comparison in terms of voltage gain and voltage stress are quadratic boost converter, Boost converter with voltage multiplier cell [7], Hybrid POEL converter with self switched inductor cell and double self switched inductor cell [15]. The reason for selecting POEL Switched inductor (SI) converter for comparison is the similarity in the number of inductors and diodes in the proposed converter. Proposed converter is the modified version of quadratic boost converter by voltage multiplier (VM) cell. Thus quadratic boost converter and Boost converter with VM cell [7] are taken for comparison.

Table 3 Comparison of proposed converter with few high voltage gain converters

<table>
<thead>
<tr>
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<tbody>
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<td>1</td>
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<tr>
<td>2</td>
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<td>5</td>
<td></td>
<td>8</td>
<td>12</td>
<td>14</td>
<td>15</td>
</tr>
<tr>
<td>6</td>
<td>Voltage gain(Vg) ($\frac{1}{(1-D)}$)</td>
<td>$\frac{M+1}{1-D}$</td>
<td>$\frac{2D}{1-D}$</td>
<td>$\frac{3-D}{1-D}$</td>
<td>$\frac{M+1}{1-D}$</td>
</tr>
<tr>
<td>7</td>
<td>Duty cycle</td>
<td>0.3</td>
<td>0.7</td>
<td>0.3</td>
<td>0.5</td>
</tr>
<tr>
<td>8</td>
<td>Gain ($\frac{V_o}{V_i}$)</td>
<td>2.04</td>
<td>13.1</td>
<td>2.85</td>
<td>4</td>
</tr>
<tr>
<td>9</td>
<td>Voltage stress of switch</td>
<td>$V_o$</td>
<td>$\frac{V_o}{M+1}$</td>
<td>$\frac{V_o}{1-D}$</td>
<td>$\frac{V_o}{M+1}$</td>
</tr>
<tr>
<td>10</td>
<td>Voltage stress across output diode</td>
<td>$V_o$</td>
<td>$\frac{V_o}{M+1}$</td>
<td>$\frac{V_o}{1-D}$</td>
<td>$\frac{V_o}{M+1}$</td>
</tr>
</tbody>
</table>

$V_o = 40V$, $V_i = 12V$, $V_{in} = 36V$

11 Duty cycle 0.64 0.75 0.8 0.78 0.5

12
Voltage gain versus duty cycle of proposed converter and compared with converters in [15], quadratic and boost converter with VM cell [7].

Semiconductor devices voltage stress versus voltage gains of proposed converter and compared with converters in [15], quadratic and boost converter with VM cell[7].
Table 4 Comparison of component utilization of proposed converter with conventional converter

<table>
<thead>
<tr>
<th>No</th>
<th>Component Utilization</th>
<th>Proposed converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Duty cycle</td>
<td>0.64</td>
</tr>
<tr>
<td>2</td>
<td>SUF Switch Utilization Factor</td>
<td>0.75</td>
</tr>
<tr>
<td>3</td>
<td>No of switch</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>DUF Total Diode Utilization Factor</td>
<td>0.5</td>
</tr>
<tr>
<td>5</td>
<td>Total no of diode</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>DUF</td>
<td>0.1166</td>
</tr>
<tr>
<td>7</td>
<td>Inductors</td>
<td>0.1197mH</td>
</tr>
<tr>
<td>8</td>
<td>( i_{in} )</td>
<td>3.32A</td>
</tr>
<tr>
<td>9</td>
<td>Total energy volume/inductor</td>
<td>3.31A</td>
</tr>
</tbody>
</table>

The comparison in Table 3 and Table 4 are performed with \( P = 40W \), \( V_g = 12V \), \( V_O = 96V \) and \( f_s = 60kHz \) and the results of the comparison are concluded as follows:

6.1 Static gain

Table 3 shows the comparison of proposed converter with Voltage lift converter [15], Quadratic boost and Boost converter with voltage multiplier cell [7]. Fig 4 shows the graphical comparison of voltage gain between converters. One can see the proposed converter has high voltage gain compared to other converters taken for comparison. It is found that voltage conversion ratio is about 22 times that of the line voltage for the duty cycle 0.7.

6.2 Main switch and output diode voltage stress

From the table 3 comparative study on voltage stress on switch and output diode for proposed converter with other converters are made. Fig 5 presents the graphical comparison of switch voltage, multiplier and output diode voltage stress of the proposed converter. The switch and output diode voltage stress depends on number of multiplier cell. By increasing the multiplier cell, the voltage stress
on the semiconductor devices can be reduced severely.

6.3 Switch/Diode utilization factor

Table 4 illustrates the comparison of switch and diode utilization factor of proposed converter with quadratic boost converter and boost converter with voltage multiplier cell [7]. Switch utilization factor is found to be high in the proposed converter. Due to increase in number of diode, total diode utilization factor slightly less compared to boost converter with voltage multiplier cell. Total energy volume of inductor of the proposed converter is slightly high compared to other converter.

7 Simulated and experimental results

The proposed converter is tested with 40W prototype to verify the theoretical analysis. The electrical specifications are $P_O = 40W$, $V_g = 12V$, $V_O = 96V$, $I_S = 50kHz$ and $R_L = 230\Omega$. Inductor $L_1$, $L_2$ and $L_r$ is chosen as 0.119mH, 0.239mH and 0.5uH respectively. Input and output capacitors are selected as 22uFas per equation 16. Voltage multiplier capacitor is selected as 0.5uf from the equation 17. Fig 6 is the photograph of the converter implemented in the laboratory. Simulation is carried out in nI5 simulator. Fig 7(a)-(d) shows the simulated waveform of the voltage across the multiplier diode, output diode, multiplier capacitor voltage and inductor current. Fig 8(a) shows the main switch stress voltage is 47V for the output voltage of 95V. Fig 8(b) presents the voltage across the multiplier diode which is equal to 49V for the output voltage of 95V. Fig 8(c) shows experimental output diode stress voltage of 49V which is very less compared to quadratic boost converter where the switch and output diode stress voltage is equal to output voltage. Fig 8(d) presents the multiplier capacitor voltage and is equal to $V_O / M + 1$. From Fig 8(a)-(c) one can see that the voltage stress across switch and other diodes depend on the number of multiplier cell and the expression to the maximum voltage stress on different components in the converter is given in table 2 which matches with the experimental results.
Figure 6: Photograph of the hardware implementation of the introduced converter

Figure 7: Simulated results (a) Multiplier diode and Output diode stress voltage (b) output voltage (c) multiplier capacitor voltage (d) Inductor current.
Figure 8 Experimental results. (a) Output voltage and switch voltage for D=0.5 (X-scale: 10us/div, CH1 : Y-scale: 30V/div, CH2 : 100V/div) (b) Voltage multiplier diode voltage stress and output voltage for D=0.5 (X-scale: 10us/div, CH1 : Y-scale: 30V/div, CH2 : 45V/div) (c) Output diode voltage stress (X-scale: 10us/div, Y-scale: 45V/div) (d) Voltage Multiplier capacitor voltage(X-scale: 10us/div, Y-scale: 25V/div)

8 Conclusion

A non-isolated DC - DC converter is constructed by integrating quadratic boost converter with voltage multiplier cell. The proposed converter possesses an input inductor so the input current is ripple free. And, hence such a converter is suitable for fuel cell application where the ripple free input current is needed. The features of this converter include high voltage conversion ratio, low voltage
stress on the semiconductor devices and high efficiency. This converter employs just a single active switch, can operate with simple control circuit and structure of the converter is simple. The measured efficiency is found to be 88% at half-load.

References


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