

Designing of 2-D reconfigurable fabric architecture for edge detection techniques

Manisha Khorgade¹ and Pravin Dakhole²

¹Research Scholar, YCCE, Nagpur, India

manisha.khorgade@gmail.com

²Professor, YCCE, Nagpur, India

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Abstract

Recently multimedia, wireless applications increasing complexity which is motivation for the system designers to innovate continuously. Balancing performance metrics challenges while designing complex system. The strongly evolving class, Coarse - Grained Re - configurable Architecture (CGRA) is presently getting attention and performed excellently through flexibility in fabrication. There is large range of components still existing for system building blocks as choices. The Reconfigurable fabric (RF) is presented as an important building block design of CGRA processor. A new design of reconfigurable fabric(RF) to achieve parallel processing techniques is proposed here. RF contains set of processing elements(PE) for 2 dimensional processing. These functional blocks are arranged in mesh type of arrangement. This implemented design is analyzed using image edge detection technique for various system parameters like power, processing speed and area using various FPGAs.

Key Words : CGRA, Processing Element, Reconfigurable Fabric, Mesh type Modelling, FPGA, Image Processing

1 Introduction

Increasing complexity of wireless and multimedia applications are driving the system designers to innovate continuously. A fundamental trade-off between flexibility and the traditional performance metrics (energy-area-timing) is being deemed important than ever. In such a scenario, the building blocks of modern System-on-Chip (SoC) - under critical review are those with a tunable balance of performance and flexibility. Coarse-Grained Reconfigurable Architecture (CGRA), with strong performance advantage as well as ability to be flexed post fabrication, is one such key building block. Recent design proposals, both academic and commercial, includes CGRAs for DSP applications [1] [2] [3] or are completely based upon CGRAs [4] [5]. Since the traditional application of FPGAs is mostly restricted to prototyping and emulation, design methodology of CGRAs is still an emerging field. As the defining roles of CGRAs in modern systems are getting clearer, design flows are being proposed. Regardless of the approach followed by these design flows, the central challenges of design remain same.

1.1 Modeling

1. Most of the research in the field of CGRA design are focused on parameterize design space exploration rather than on high-level modeling. The physical implementations in most cases are done earlier due to the limitation of aggressive automatic physical optimization or lack of re-targetable CGRA mapping and placement-routing tools. Commercial FPGA vendors have suggested RTL abstraction as a level of modelling, though only for simulation purposes. As a result, the modeling platforms either provide limited flexibility of modelling or are completely lacking of implementation aspects. The recently proposed ADRES architecture, allows changing the parameters like - number and size of register file associated with each basic functional unit, operation set supported by the functional units and interconnect topology of its reconfigurable array. The limitation of such a parameterize way is that, the introduction of a novel design parameter might lead to serious modification in the associated tool-chain.

1.2 Mapping, Placement and Routing

Mapping, placement and routing (referred together as CGRA synthesis in future) are three important phases of porting a data path to a CGRA. In several attempts to perform CGRA synthesis, the architecture is partly or completely fixed. However, that may not affect the liberty of synthesis algorithms. A completely innovative approach for exploring the functional units of a RF using mesh-based topology in CGRA with corresponding mapping algorithm is presented in this paper.

The main part of RF unit is functional unit. It is like ALU. In this designing approach, it is considered as processing element(PE). There are various types of placement and routing techniques of reconfigurable fabric unit and processing element. In this paper we will discuss implementation of RF using Mesh type topology to analyze area, time, throughput and speed for edge detection technique. Paper contains methodology for implementation in section 2, similarly section 3 and 4 will give implementation of PE and RF unit. Section 5 contains operation of system and analysis is studied and results are contained in section 6. Section 7 contains conclusion and after that references.

2 Methodology

The reconfiguration system of DSP processor architecture can be implemented using software and hardware techniques. Reconfigurable architecture has two types as coarse grained (CGRA) and fine grained (FGRA). CGRA works with byte wise input and FGRA works with bitwise input. Each of it is having its own advantages as well as disadvantages. Here we are considering CGRA which has reconfigurable fabric (RF) along with control unit and input and output unit.

The RF has the set of processing elements(PE). They are arranged with mesh type of topology. Here PEs are the homogeneous type. It accepts n-bit stream of inputs and n-bit stream of outputs. PEs can be arranged in other type of arrangements also like bus, crossbar. The main task is to schedule given task and distribute it among all PE to perform. During instruction scheduling, a record is maintained to keep track of which resources are used in each time

slot. Considering that the scheduler for a CGRA must perform placement of operations, routing information should be recorded by the scheduler. This routing information can be included in the table because PEs are used both for computation and routing. So that parallelism can be achieved and scaling with various applications.

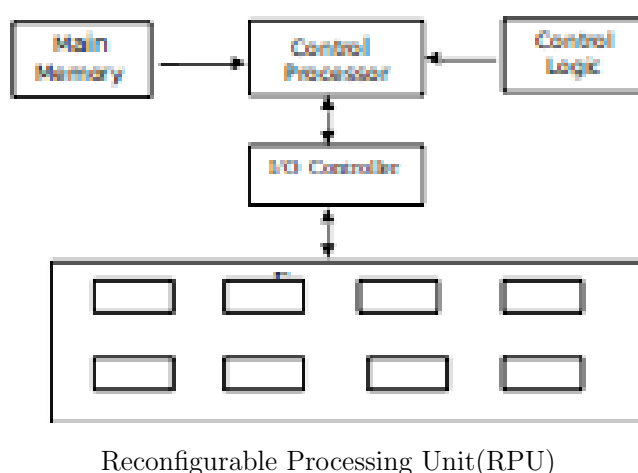


Figure 1: Block diagram of Reconfigurable Processor

In this approach task has been divided and feed into 2×8 arrangement of PEs to achieve parallelism. For observing results of this arrangement various applications like image processing having edge detection technique with sobel operator is performed.

3 Implementation of PE

The processing element is the heart of RF unit. They are designed like a RISC. It performs the task for particular application send by control unit. PE is designed like RISC processor to perform certain task like ALU. It is RF unit performing set of functions ask to perform..This PE is taking 8 bit input and 8 bit output, PE is 8 bit. The designing is optimized in such a way that input-output stream can be change into 16 bit,32 bit,64 bit and so on .But it will change processing time and speed of operation. As bit size

increases, processing time, speed also increases. Each PE contain input(bit stream),output(bit stream),clock, enable and operation to perform. PE has 2K RAM memory to store bit for small task and task is perform parallel to optimize time and speed. The RTL View of PE is given as follows which define the input and output stream with enable, clock also. The RTL View of PE is given as follows which define the input and output stream with enable, clock also. The RTL View of PE is given as follows which define the input and output stream with enable, clock also.

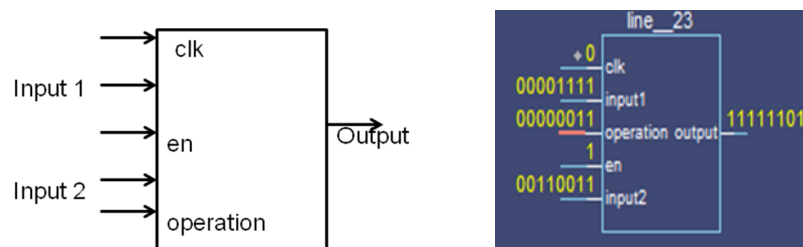


Figure 2: (a) Block diagram of Processing Element (b) RTL View of Processing Element

4 Implementation of Reconfigurable Fabric

Reconfiguration means multiple PEs are arranged with their different types of arrangement to perform various tasks at same time .If the decision about reconfiguration is done before running program ,that reconfiguration technique is considered to be static reconfiguration. In this approach 8 PEs,4 PEU and 2 Nodes to control logic are designed. The granularity is coarse grain type with mesh type of arrangement s shown in fig 4(a) and 3 (b)also . Mesh-based architectures arrange their processing elements in a rectangular array, featuring horizontal and vertical connections. This structure allows efficient parallelism and a good use of communication resources. However, the advantages of a mesh are traded for the need of an efficient placement and routing step. The quality of this step can have a remarkable impact on the application performance. It

is a homogeneous type of reconfigurable component i.e. even granularity.

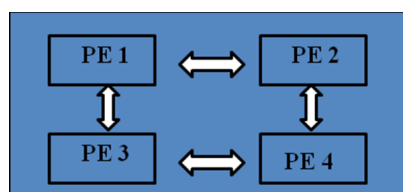
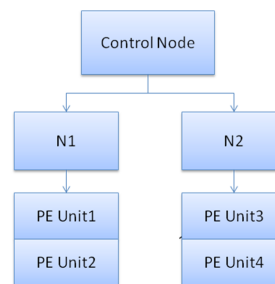


Figure 3: (a) Mesh type arrangement of RF



(b) Design of proposed RF Unit

Depending on the requirement of PEs as per task, scale-in and scale-out of unit decision taken by control node. With the help of this control unit, various applications can be run simultaneously, so with this reconfiguration is also achieved.

4.1 Implementation with Image processing

This arrangement uses Edge detection operation of the image using sobel operator. This method uses both x-direction $g(x)$ and y-direction $g(y)$ operation of masking. Finally, it gives output with $g(x) + g(y)$ with masking matrix as shown in fig 4(b). Let us assume

$$G(x) = [16*16] * [x\text{-operator}] = \text{Val 1} ;$$

$$G(y) = [16*16] * [y\text{-operator}] = \text{Val 2};$$

$$\text{Output pixel} = \text{Val 1} + \text{Val 2}$$

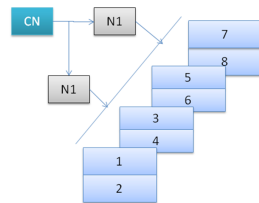


Figure 4: (a) Internal connectivity of proposed RF Unit

X operator			Y Operator		
G(x)			G(y)		
1	2	1	-1	0	1
0	0	0	-2	0	2
-1	-2	-1	-1	0	1

(b) Sobel Operator

5 Operation

Here we have 3 bit operation mode (B2B1B0) to perform depending upon the values of bits from MSB (B2) LSB (B0). For selection of controller C1 and C2, B2 (MSB) is selected. It means value of MSB decides which controller is selected. If the value of B2 is 0, controller C1 is selected and if B2 is 1, Controller C1 and C2 are selected. C1 has 2 PEU. Each and PEU has 2 PES, similar with C2 also. So if C1 selected, it will select 2PEU with 4 PEs. If C1 and C2 are selected, it will select 4 PEU with 8 PEs. If B1 bit is selected and bit is 0, C2 is selected which select PEU0 (2 PEs). If B1 is 1, C2 is selected which select PEU0 and PEU 1 (4 PEs). For third bit (B0), it will select controller C1. If B0 is 0, C1 is selected with PEU0 (2 PEs) and if B0 is 1, it will select PEU0, PEU1 (4 PEs).

Table 1. Bitwise distribution with controller, PEU & PE selection

Bit	Bit Value	Controller	PEU	PEs
B2	0	C1	--	--
	1	C1 & C2		
B1	0	C2	PEU0	2
	1	C2	PEU0, PEU1	4
B0	0	C1	PEU0	2
	1	C1	PEU0, PEU1	4

6 Results

1. The design is implemented and evaluate for image processing application with edge detection technique using sobel operator. Processing is done for various image sizes like 16×16 , 32×32 , 64×64 , 128×128 for 8 bit input and 8 bit output. Various parameters are considered for evaluations are time, area, power, speed and throughput. Power & speed (Image Size 64×64). The pixel value below threshold value ,it will be remaining same but if pixel value is above threshold value ,it will become zero, shown in fig below.

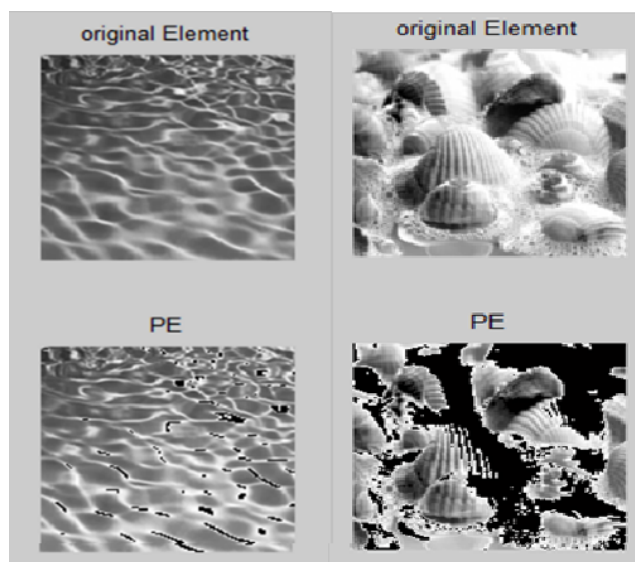


Figure 5: (a) Image processing results with RF

These various images are processed and retrieved from RF after processing. The result obtained are as shown in fig.5(a) for the images before processing and image after processed with edge detection for proposed design. For this proposed design, area required and delay time is comparatively less than Linear dimensional Reconfigurable array .The pixel value below threshold value ,it will be remaining same but if pixel value is above threshold value ,it will become zero, shown in fig 5(a).Various parameters of systems are evaluated like power, speed and processing time for different

image size for optimization of design. As design is 2-d, it will be processing image using set of 2 PEs or more PEs for row wise and column wise. This way parallel processing will be computed and time required will be less as shown in Table 3, Table 4.

Table. 3. Analysis of input given and power, speed

clk	Input	Power (mW)	Speed
1	000	0.3	Speed up by 98%
2	001,100	0.5	
3	101,110	0.8	
4	111	0.11	

Table .4. Processing time with number of PE used

Case	NO of controller	No of PES	Image size 16*16 Time(ms)	Image size 64*64 Time(ms)	Image size 128*128 Time(ms)
000	1	2	0.7352	14.415	59.535
001	1	4	0.2706	5.256	21.697
100	2	4	0.3677	7.207	29.767
101	2	6	0.3677	7.207	29.767
110	2	6	0.1354	2.628	10.848
111	2	8	0.1354	2.628	10.848

The area parameters are also monitor using various Field programmable gate array (FPGA) devices to optimize the design. The following table gives detail review on area parameter of FPGA like slice register, LUTs, logic used, IOBs maximum period and frequency is also observed. The frequency almost same for all FPGA. In hardware implementation our system is also working more effectively and efficiently for image processing with these parameters from table shown below.

Table. 5. Area considering various devices for image 128*128

Device	Spartan6-XC6SLX100T	Spartan6-XC6SLX75T	Spartan 3E
Speed grade	-3	-3	-5
Flip flops	4672	4760	4540
Slice LUTs	6850(10%)	6850(14%)	4610
Slice registers	4558(3%)	4558(4%)	13133
Logic used	6850(10%)	6850(14%)	4610
IOBs	4101	4101	4101
Max period	6.263ns	6.236ns	15.765ns
Max Frequency	159.678 MHz	159.678MHz	63.43Mhz

7 Conclusion

A novel approach design of reconfigurable fabric of reconfigurable processor is offered in this paper. In particular, since reconfigurable computing is developed as a vast discipline and so it demands separate attention to the sub disciplines such as reconfigurable processors. Edge detection technique in image processing is used to analyze and tried to optimize design with various parameters like area, speed, time, power and throughput. Anticipating the future challenges, several research directions are optimization of PE, RF with these parameters and many others. It is likely that our understanding of SoC architectures will evolve with time. The design will be apply for other application like communications, cryptography image/video decoding which give reconfiguration and scalability also.

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