

Design of Dynamic Latched Comparator with Reduced Kickback Noise

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Abstract

Dynamic latched comparators are used because they use two back-to-back cross coupled inverters to convert a small input voltage difference to a supply voltage level in a short time, which is known as positive feedback technique. Here we adopted a technique to reduce kickback noise produced by regenerative nodes of dynamic comparator. Our reduction technique uses Exclusive OR gate in between regenerative nodes and inputs which will avoid to interfere inputs with noise. To present our results with existing systems we used Mentor Graphic Tool for simulation purpose. The proposed design can be used for the application of SAR ADC in Implantable Biomedical Devices.

Key Words : Kickback noise, Positive feedback technique, Successive Approximation Register (SAR) Analog to Digital Converter (ADC).

1 INTRODUCTION

Analog to Digital Converters (ADC), like Flash ADC, Sigma Delta ADC, Dual Slope Converters and Successive Approximation Register (SAR), provides best applications in Electronic field that mainly deals with digital processing like Sensors, Detectors and for Biomedical engineering purposes.

Here, a dynamic comparator is designed for SAR ADC that can be used for the application of Implantable Biomedical Devices. Implantable Biomedical Devices that are used to insert inside body of human beings. Since the surgery wastes money and time, the device that is inserted in body should consume very less power and work for years without degrading its functionality.

Since Comparator components are effectively used in any ADCs, they consume more part of power produced by source that is implanted inside of human body. Therefore compared to other ADC architectures, SAR ADC has the advantage of understandable circuitry with less analog circuit network and there is a good balance between speed and cost compared to other ADCs that are available in market, mainly SAR ADCs supports scaling technology.

In order to show the results of our paper, we compared the proposed dynamic comparator with existing works and the values are tabulated with respect to Kickback noise produced by each architect and their Power dissipation also. With the help of structure of dynamic double-tail comparator shown in [1], we proposed a new dynamic double-tail comparator with additional circuitry, which can suppress the Kickback noise produced by existing dynamic comparator. Since the additional circuitry for reduction of Kickback noise consumes some part of power, the proposed dynamic double-tail comparator will consumes little bit more power compared to existing dynamic double-tail comparator.

The following sections of this paper are arranged as follows. Section II presents the operation of existing works like Clocked regenerative comparator circuits, single-tail dynamic comparator and double-tail dynamic comparator with their respective diagrams. Section III contains operation and design of our proposed dynamic double-tail comparator with kickback noise reduction circuitry. Coming to Section IV, here the Simulation results of existing and proposed comparator are presented pictorially and the comparison

value of Kickback noise and Power dissipation of respective comparator are tabulated. Finally Section V included Conclusion of the proposed work and future scope.

2 DYNAMIC COMPARATORS

Dynamic comparators are preferred to eliminate the static power consumption of normal comparator. Since dynamic comparator works with respect to clock, power consumption of dynamic comparator is less compared to normal comparator that is if the comparator does not uses any clock. In order to provide perfect output logics dynamic comparator uses latch circuitry designed with two inverters which coupled in back-to-back. To evaluate the performance of any comparator, its parametric characteristics like power dissipation [2], offset voltage [3], random noise [4], leakage currents [7] and kickback noise [5],[11] are mainly considered into account of design considerations. Here, the operations of existing dynamic comparators are presented with their advantages and disadvantages.

A. Single-tail Dynamic Comparator

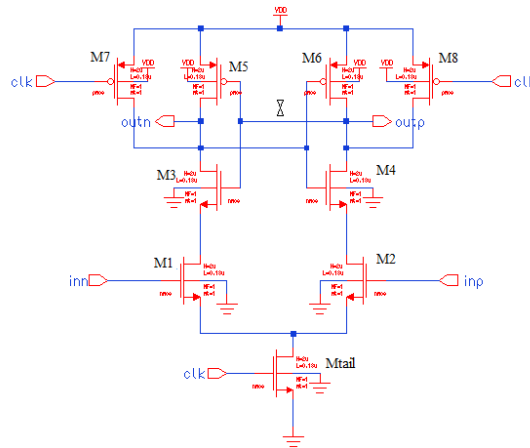


Figure 1: Schematic diagram of Single-tail Dynamic Comparator

The circuit diagram of the Single-tail dynamic comparator [11] is shown in Fig. 1. The circuit functionality is as follows. When $\text{clk}=0$ (Low), then comparator will be in reset phase. This is also called pre-charge phase. In this phase, the outputs of comparator i.e., outn and outp will charged to level of supply voltage (V_{DD}). Similarly, when $\text{clk}=1$ (High), the comparator will be in Comparison phase or evaluation phase. Here, based on inputs we are giving to comparator i.e., inn and inp the outputs of comparator will discharge. That is, if $\text{inn} < \text{inp}$, then the output coupled with inn will discharge to ground fastly compared to the other output. Suppose if $\text{inn} > \text{inp}$ then, the output coupled with inp will discharge to ground fastly compared to the other output discharge interval. Coming to its advantages, it has high input impedance and low power dissipation compared to other comparator circuits. Coming to its disadvantages, it suffers with latch delay and the inputs are largely disturbed with Kickback noise that is generated by positive feedback latch circuitry from output nodes of comparator.

B. Double-tail Dynamic Comparator

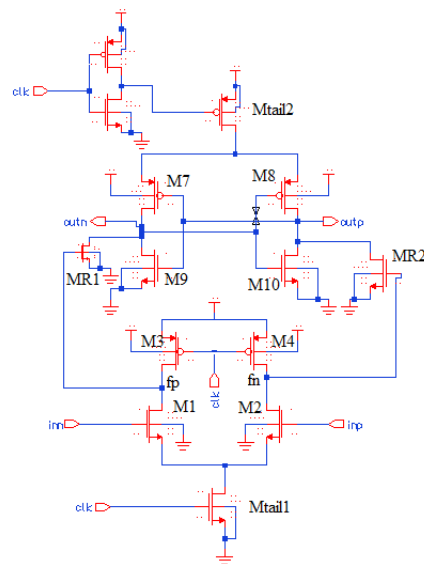


Figure 2: Schematic diagram of Double-tail Dynamic Comparator

The circuit diagram of double-tail comparator [11] is shown in Fig. 2. The functionality of this circuit is same as single-tail dynamic comparator expect, in this circuit the latch circuitry is separated from the differential amplifier circuitry and different supply voltage is used for both latch circuit and differential amplifier circuit. It has the advantage of reduced Kickback noise compared to single-tail dynamic comparator. Coming to its disadvantages it has more number of transistors and requires additional supply voltage than single-tail dynamic comparator. Since the number of transistors increases than single-tail dynamic comparator its power dissipation also increases.

C. Kickback noise

If the design fails to provide perfect load at the output terminals, then some sort of disturbance will produce the latch circuit and that disturbance will feedback to comparator inputs. Therefore the inputs will interfere with noise from the output nodes and its actual inputs may vary because of disturbances and also its output functionally will effect drastically and gives incorrect values as output. Here the disturbance from the positive feedback latch that is interfered with inputs is known as Kickback noise.

The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

3 DOUBLE-TAIL DYNAMIC COMPARATOR WITH KICKBACK NOISE REDUCTION TECHNIQUE

Since the double-tail dynamic comparator has less kickback noise compared to single-tail dynamic comparator, here we adopted the architecture of double-tail comparator and the technique to reduce the kickback is implemented to it. For the reduction of kickback noise we added an Exclusive OR gate in between the positive feedback latch circuitry and comparator inputs. And also to avoid the interference of the noise with inputs of comparator additional switches S1, S2 and S3 are used as shown in fig. 3.

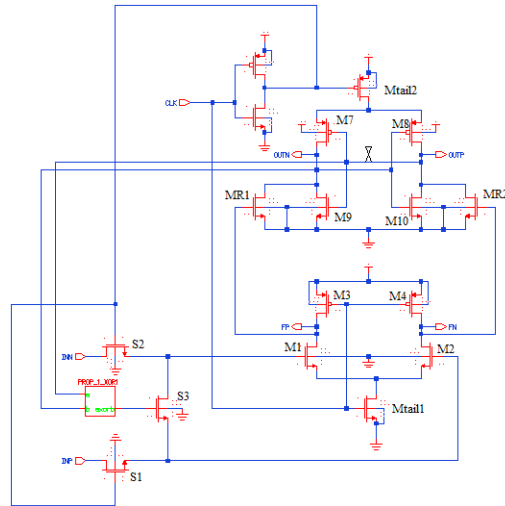


Figure 3: Proposed Double-tail Dynamic Comparator with Kick-back noise reduction technique

Our new design also works as same as existing comparators but the only difference is switches and Exclusive OR gate implementation. While coming to its operation, in reset phase($\text{clk}=0$), the switches S1 and S2 will be ON condition and the transistor M1 and M2 will precharged to its input voltage from inn and inp. And the outputs outn and outp will be precharged VDD. In case of comparison phase($\text{clk}=1$) the switches S1 and S2 will be in OFF condition, therefore the inputs inn and inp will be disconnected to differential amplifier circuit, in this way it avoid interfering the inputs with disturbances from the positive feedback latch circuitry. Therefore the kickback noise is suppressed because until the outputs discharged to ground no inputs will allow connecting with differential amplifier stage. Initially S3 switch will be in OFF condition because no charge at the output nodes of comparator. After that it functions with respect to Exclusive OR gate where the outputs of comparator are given as input to Exclusive OR gate and Exclusive OR gate output is given as input to switch S3.

4 SIMULATION RESULTS

Finally, both existing designs and proposed design is simulated using Mentor Graphics Tool with 130 Nanometer technologies. And their results are compared and values are tabulated. For simulation of all designs we used 1V as the supply voltage.

Table 1: Performance Comparison

Comparator Structure	Power Dissipation	Kickback Noise
Conventional Single-tail dynamic comparator	604.8654 pW	1766.0834 V
Conventional Double-tail dynamic comparator	1.0049 nW	526.0242 V
Proposed Double-tail dynamic comparator	3.6585 nW	85.3582 V

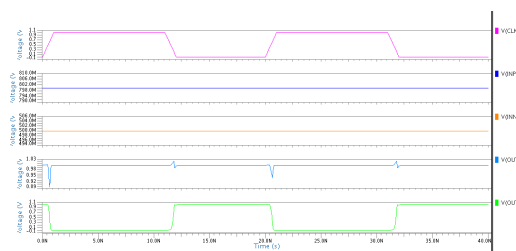


Figure 4: Transient response of Single-tail Dynamic Comparator

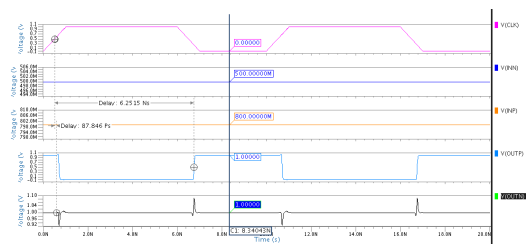


Figure 5: Transient response of Double-tail dynamic comparator

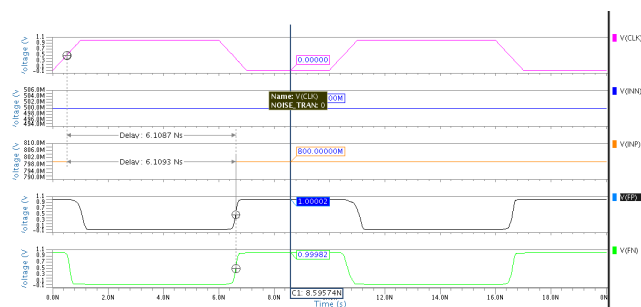


Figure 6: Transient response of new Double-tail dynamic comparator with reduced kickback noise

5 CONCLUSION

In this paper, we presented a new double-tail dynamic comparator which has reduced kickback noise. Since some additional circuitry is need for the reduction of kickback noise, it consumes some additional power compared to existing double-tail comparator.

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