

Design of an Interconnection Network using VLSI Photonics: Issues and Challenges

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Abstract

This paper addresses a newly emerging frontier technology called VLSI photonics. It is a new field of optical circuit or optical network technology rapidly evolving in micro/nano-scale. It discusses the science and engineering of micro/nano-photonics and integration that can lead to VLSI photonic circuits and networks of generic and application-specific nature. The world is facing many new kinds of problems like increasing demand for big data, higher information capacity, increasing population, increasing cost of energy, shortage of food and natural resources, environmental problems, global warming, increasing medical and health problems, and increasing demand for well living. Photon-based technology, on the other hand, is showing many new promises that can lead to solutions to many of these problems that electrons alone cannot. Compact, high-speed, light-weight, and low-powered optical and photonic micro/nano-systems using nano-wires, micro/nano-structures, plasmon-

ics, and meta materials, assure of new properties and functions that can provide new solutions for the rising problems, that can address green and sustainable IT/BT/NT applications in this century. The new optical systems consist of arrays of micro / nano-scale optical wires, circuits as well as devices on chips or on modular boards to perform the functions of sensing, switching, modulating, processing, transporting, routing, and distributing optical signals. The optical components consist of micro/nano-scale light sources, waveguides, detectors, switches, modulators, sensors, couplers, filters, resonators, plasmonics devices, and quantum structures, made of polymer, silicon and other semiconductor micro/nano-materials.

We discuss scientific and technological issues and challenges for the smallness and integration of micro/nano-scale photonic materials, devices, circuits, and networks for ultra-small and high-density integration and application. It includes new physics, theories, materials, designs, and structures. New perspectives and visions will be discussed by the side of with the historical perspectives of the electrical technology. Recent progresses and examples will be presented.

Key Words and Phrases: nirgan software; Photonics; opt- electronics ;photonic density

1 Introduction

Over the last 15 years, the optoelectronic area has witnessed a stable drive towards the full addition of optoelectronic components inside their associated VLSI electronic processing circuitry. This style, formerly fuelled by the long-haul telecommunications industry was geared towards the fabrication of OEICs (Opto-Electronic Integrated Circuits). More recently, the need for more collective data bandwidth in optical information dealing out systems has initiate numerous industrial and educational re- search in the design and construct of inter-board, inter and intra chip interconnection schemes. The resulting devices called smart pixels or optoelectronics-VLSI components, advantage from the strengths of optics in data transmission (massive I/O photonic density, defense to electromagnetic meddling, large fan-out capability, routine impedance

matching, power savings at long distance, real-time re-congurability) and the processing power of VLSI electronic circuits. Today, demonstrators based on this technology display the same aggregate bandwidth as that foreseen among electronic systems for the year 2007. This remarkable achievement is rendered possible by a variety of factor:1 The combination of micron-size optoelectronic transceivers among VLSI circuits;2 the massive parallelism accessible by free-space optics;3 a healthier understanding of the added-value of optics in information processing systems; and (4) the growth in low-cost optical assemblage, testing and pack- aging. In all these domains, yet, technological issues ruin the full latent of this technology: (1) the interface of optoelectronics among silicon-based VLSI circuits is still technologically undeveloped; (2) the arrangement and fabrication limitations faced by free-space optical mechanism might be bettered by the acceptance of obtainable solutions and established standards; (3) the sluggish progress in adopting optics in computer architecture is suggestive of the common need of information of optics by computer scientists as well as the unawareness of computer science by optical engineers;4 the complexity in assembling and testing completely functional prototypes is due to the necessity of feeding a vast amount of vector tests; as well as (5) the inter-disciplinary nature of common systems require large teams of experts with different educational background.

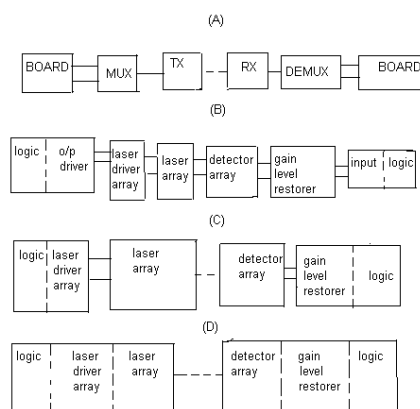


Fig 1. Historical perspective in optical interconnection

In Optical information processing systems (solid line represents electronic connections, broken lines represents optical connection. In fig 1. (A) and (B)was originally encountered in long haul telecommunications and (C)and(D) is generations of VLSI opto-electronic systems which are actively researched.

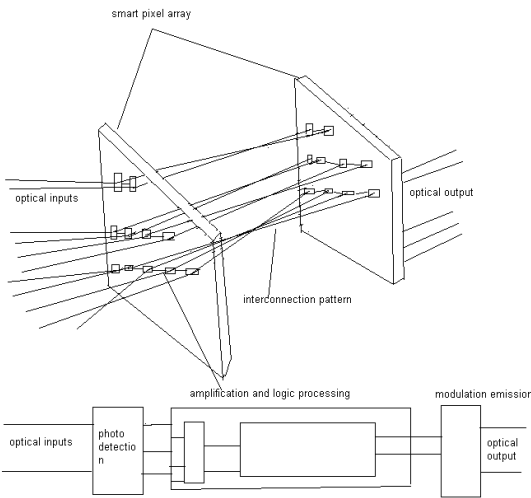


Fig 2. Smart pixel array and detailed smart pixel array diagram

Fig 3 shows the clear picture of technologies used worldwide in optoelectronics. And Fig 4.shows the smart-demonstrators classification in terms of logic complexity and functionality.

Group and demonstrator system	Input array	Electronic logic family	Output array
Lucent Technologies (switching chips)	GaAs PIN diodes	Si-CMOS	GaAs MQW modulators
Heriot-Watt University (bitonic sorter/crossbar)	InGaAs PIN diodes	Si-CMOS	InGaAs modulators, GaAs VCSELs
MIT (optical neural network)	MSM-GaAs	Direct Coupled FET Logic	Epitaxy on Electronics GaAs/InGaP LED
McGill University (optical backplane)	GaAs PIN diodes	Si-CMOS	GaAs MQW modulators
Georgia Tech (ADC converter)	MSM-GaAs	Si-CMOS	Not applicable
UC Boulder (board to board pipeline)	MSM GaAs	Si-CMOS	GaAs VCSEL
University of Edinburgh (intelligent display)	Not applicable	Si-CMOS	Liquid crystal display on silicon
UC San Diego (optical transpose interconnect system)	MSM GaAs	Si-CMOS	GaAs VCSEL

Fig 3. Examples of techonologies used worldwide in optoelectronics-VLSI system

Logic complexity	Functionality	Research group
Photodetection	Thermal imaging	Commercial use
Primitive operations	Artificial retina	Institut d'Optique Applique (France)
Routing	Optical crossbar/sorter switch matrix	Heriot-Watt (Scotland), Lucent Technologies (USA), McGill University (Canada)
SIMD processor	Systolic processor	Georgia Tech (USA)
ADC	Image processor	Georgia Tech (USA) United States Military Academy (USA)

Fig 4. A classification of some smart-demonstrators in terms of logic complexity and functionality

2 Optoelectronic-VLSI benefit from several advantages

1. The design and manufacture of high-aggregate bandwidth systems is enabled through the huge parallelism of the dense space-multiplexed array of optoelectronic components.
2. A lesser charge of interconnect is so permitted by the optical attend to the transceivers in the third dimension. The shift to higher pin-count is consequently facilitated.
3. The partitioning into split domains (electrical and optical) of signal with power supply (and ground) I:Os eases the lessening of electronic crosstalk and switching noise.
4. Data-acquisition as well as data addressing to further hardware (such as optical memoirs) can be parallel.
5. The power consumption of off-chip interconnections is worse than for terminated wires due to the intrinsic impedance matching of optical terminations. For example 30% savings of on-chip power rakishness, compared to an all-electronic version, has been demonstrated by the utilization of an optical distribution idea.
6. The worldwide optical distribution of a clock allows the configuration of isochronous regions inside a wire-limited VLSI chip. This property could permit the design of low access time DRAMS.
7. The reconfiguration of non-local, space-variant interconnects patterns become possible on a single-cycle timescale, allowing

so greater freedom in the design of extra efficient computer architectures and algorithms.

8. Significant savings in shielding cost of the electronic equipment are rendered likely from the time when the optical transmission of information does not undermine the signal integrity

3 VLSI components Opto Electronics

Every smart-pixel devices, irrespective of their fundamental electronic logic family and optoelectronic boundary, receive, adjust or emit information in the optical area and process it in the electronic domain. Physical and schematics function of a generic smart-pixel. Optical data streams are input into one or more than a few photo detectors, which convert the beam concentration into photocurrent. Most optical schemes rely on binary intensity modulation. The rehabilitated current signals are after that amplified (either by a current or a voltage amplifier) and processed electronically. The resulting out- put data drive modulators (voltage difference) or emissive devices (current difference). Most of the exam- pled modulators, currently, are based on many quantum well structures and exploit the quantum confined stark effect. Photo detectors contain the similar class of modulators used as PIN photodiodes, metalsemi- conductormetal (MSM) detectors or photoconductive devices. The emissive devices can also be light emitting diodes (LEDS) or, more frequently, vertical cavity surface emitting lasers (VCSELs). Emitters, modulators and photo detectors can be fabricated on the same substrate, which is usually unlike from the silicon substrate loyal to electronic processing. As a result some interfacing technique is needed to join the optoelectronic inputs to their electronic counterparts. In the follow of full integration, a further lenslet or hologram array can exist fabricated or inter- faced on top of the electronic chip in order to collimate or guide the inward and outgoing optical beams. The amplification stage is typically not noise-limited and ranges from the simple but capacitance-limited voltage gain amplifier, the trans-impedance amplifier and some variations from it to the sophisticated charge or current-sensed amplifier. Arrays of perhaps up to 104 (usually) matching pixels, occupying roughly the same chip area as the original electronic chip, are interconnected to

other chips using free-space or guided wave optics even as logic and local on-chip interconnection is electrical. The logical processing stage is typically devoid of R3 (recovery, retiming, reshape) electronic circuitry because of the limited amount of silicon real estate at each pixel. The amount of electronic gates per pixel dictates the neatness, i.e. the logic complication of the protester. The electronic logic families can variety from GaAs-based direct coupled FET-logic to standard Si-CMOS as shown in Table 1. The tasks performed by some of the demonstrators variety from primitive image operations such as noise elimination to extra complex functions such as systolic processing some of the design challenges are

- Device Integration and Interface issue
Far above the ground bit-rates and low power consumption shoot from the technological progress prepared by the devices themselves as well as the electronic drivers . The Although the MQW modulator offers the most excellent performance in terms of power dissipated and optical switching energy, the fast technological progress in VCSELs operating frequency (multi Gbit) and threshold current (sub mA) is likely to render this benefit obsolete. The complexity in monolithically integrating emitters onto silicon requires utilization of hybrid skill if the electronic processing is not approved out on IIIV semiconductor based chip.
- System Integration issue
The option of optical transceivers motivation depends eventually on the application and the system volume. For example the short number of VCSELs that can be place on a chip nowadays (around 64), due to electrical crosstalk and driving ability confines the parallelism of channels even though the fan-out performance of such devices is excellent. On the other hand, two main drawbacks in modulator based systems is necessitate for an outside laser source to read the devices and the requirement to have large voltage swing in arrange to drive them. On the other hand, VCSEL-based demonstrators have yet to show fully prepared arrays of more than 64 devices, all running at a number of GH.
- System assembly and testing issue

The high aggregate bandwidth of such systems is helpful only if the data to be processed be capable of fed into the system and be output on a timescale alike with the processing time of the demonstrators. Hare In the case of optical input and output data beams, the difficulty of connecting such a system to the external world lies in the focus of a hundred to a thousand optically parallel, regularly spaced channels inside a chip-compatible area. This requires exact assembly and photo mechanical have power in excess of the beams in the case of free space optics. In this specific case, a liquid prism is used to guide the beams onto specific photo detectors. Active manage feedback is provided along with the prism and the detectors. In the case of electrical input or output data streams, the difficulty lies in the frame-rate confines of the electrically addressed smart-pixel arrays appropriate to the RC-limitation of the galvanic wires and the limited number of accessible electrical pin-outs. On-board or on-chip temporary storage in the form of memory registers are needed, for which completely loaded on-chip memory banks are emptied in rupture mode into the input array during addressing are refilled, as a background action, even as the data are being processed optically. Such situation is also possible to occur for the testing of such systems as there electronic testing tools are doubtful to cope with the wonderful aggregate bandwidth generated by such systems.

4 Few mechanisms to address integration issue

As a part of our analysis, we found that there are few mechanism to address an integration issue. SoC industry is working with this mechanism since few years. Communication plays a crucial role in the design and performance of multi-core SoCs .Networks-on-chip (NoCs) has been proposed as a promising solution to simplify and optimize SoC design. On the other hand, it is predictable that improving usual communication technologies and interconnect organizations will not be sufficient to declare the need for energy-efficient and high performance interconnect fabrics, which contin-

ues to grow with each new process generation. Numerous options have been envisioned as forceful alternatives to the existing planar metal/dielectric communi qu structures. In this paper we outline the opportunities and challenges linked with three promising interconnect paradigms: three dimensional (3-D) integration, nano-phonic communication and wireless interconnect.

- 3D NoC

Three-dimensional integrated circuits offer a smart solution for overcoming the barriers to interconnect scaling, thereby offering an opportunity to continue performance improvements using CMOS technology with lesser form factor, superior integration density and the support for the understanding of mixed-technology chips. Among several 3D integration technologies, TSV (Through-Silicon-Via) approach is the most promising one and therefore is the focus of the bulk of 3D integration R&D actions. Even though both 3D integrated circuits and NoCs are proposed as alternatives for the interconnect scaling require, the challenges of combining both approaches to design three-dimensional NOCs have not been addressed until recently 5. This section gives a brief introduction on the exploration of probable architectural designs for three-dimensional NoC architectures and discusses the trade-offs among various design options

1. Symmetric NoC Router Design
2. 3D NoC-Bus Hybrid Router Design
3. True 3D Router Design
4. Multi-Layer 3D NoC Router Design
5. 3D NoC Topology Design

- Nanophotonic Interconnection Networks

The collection of growing requirements on-chip and off-chip communication bandwidths and strict limitation son the greatest on-chip temperature and power budget required by packaging constraints will make the interconnect power consumption become perhaps the most critical problem for multi-core SoC design in the predictable future. How electronic NoCs

can keep on satisfying future bandwidths and latency requirements with the chip power resources is an important open area of research.

1. Advance in Photonic NoC Components
 2. Combining Photonic NoC and 3D Integration
 3. Hybrid approach to Photonic NoC Design
- Wireless NoC
A fundamental option to the existing metal/dielectric 2-Dinterconnect infrastructures is to use transmission of signals via RF/wireless interconnects. Intra chip low latency communication can exist achieved through RF interconnects, where transmission of data is guided from end to end on-chip transmission lines. Using Frequency hand, Division Multiple Access (FDMA) with multiband frequency synthesizers and metal wires available from current CMOS processes as transmission lines a high bandwidth RF interrelate can be produced for on-chip data transport. A hybrid NoC architecture using such RF interconnects has been future. A basic wire line mesh architecture overlaid through a elevated bandwidth FDMA based RF transmission is envisioned. The RF interconnect acts as an information highway enabling quick data transport across longer distances on the chip, thus falling overall communication latency. In totaling to reduce latency, the NoC power dissipation using overlaid RF shortcuts is demonstrated to be an order of magnitude less than that in usual wire line NoCs.
1. On-Chip Antenna
 2. Network Architecture
 3. Wireless Transceiver

5 Result & Discussion

As a part of our experiment, we used NoC Simulator to find out a suitable topology. Some of these results listed here.

- Simulator used

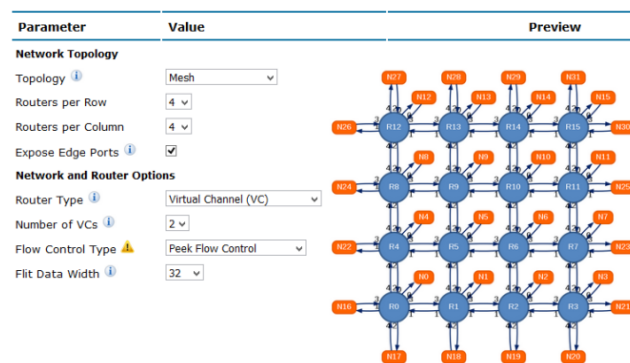
NIRGAM is a NoC simulator which is based on SystemC. Nirgam allows user plug-in and experiment with different applications and routing algorithms. And allows the user to analyze the performance (Average latency, throughput and total network power) of a NoC design for a user specified application and a user specified routing algorithm. NIRGAM simulator supports mesh, torus and mesh with link failures and irregular topologies with wormhole switching mechanism. Quality of Service (QoS) is supported where the user can reserve a specified amount of band-width for Guaranteed Throughput (GT) traffic. It allows the users to develop their own applications or they can use the available applications which are attached to the IP cores in the defined topologies. The available applications are: source (sender) application, sink (receiver) application and synthetic traffic generators (constant bit rate (CBR), bursts, and input traces based traffic). This simulator facilitates the users to include their own applications and attach them to the defined IP cores. NIRGAM is aimed primarily at the NoC research community wherein it provides researchers with convenient and efficient mechanism to experiment with NoC design in terms of routing algorithms and applications on various topologies. Users can easily plug-in their own routers and applications. The simulator is capable of dynamically loading a router and attaching any user-specified application library to any core.

- Experimental setup in Nirgam

Experimental setup is as follows

1. Mesh Topology
2. Traffic generator for 12 Gbps
3. FIFO length 32 bytes
4. Virtual channels 4
5. Packet size 20 bytes, internal flit 2 cycles
6. Clock frequency 1 GHz

- **Simulation Results**
The simulation results for average latency, average throughput and total network power with % of variation of load in uniform random traffic pattern.
- **Selected topology parameters are listed below**
The experiments are carried out to understand which is useful in order to have good bandwidth. And topology selection also depends on system complexity.



6 Conclusion

Three-dimensional integration, nanophotonic communication and on-chip wireless links are all promising alternative options to usual planar metal/dielectric-based interconnects in favor of building the communication infrastructure of future multi-core systems-on-chip. All of these rising interconnect paradigms, whose main features are summarized above, could offer remarkable advantages. However, in order to harvest their potential more researches necessary to address various challenges in many areas including system architecture, circuit design, device fabrication and CAD tool development

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