International Journal of Pure and Applied Mathematics
Volume 118 No. 11 2018, 609-617
ISSN: 1311-8080 (printed version); ISSN: 1314-3395 (on-line version)
url: http://www.ijpam.eu
doi: 10.12732/ijpam.v118i11.79
Special Issue
ijpam.eu

EXECUTION EXAMINATION OF A THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING DISTINCTIVE TRANSPORTER BASED EXCHANGING ALGORITHMS

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Abstract: As of late impressive intrigue is appeared in the utilization of Matrix Converters for mechanical drive applications. Since the origin, a few transporter based adjustment plans have been proposed for Matrix Converters. The operation and control approach of Matrix Converters is mind boggling. This paper analyzes the different balance plans for three stage AC to three stage AC matrix converters beginning from the Venturini and ideal Venturini calculation to the as of late created Sunter-Clare and Ned Mohan calculation, by displaying system. The recreation is completed utilizing PSCAD for a given info, yield, transporter exchanging recurrence and adjustment file. The recreation comes about are introduced and analyzed. The relative benefits of each calculation from the perspective of high Pinnacle Crucial esteem and low Aggregate Symphonious Mutilation for the line to nonpartisan, line to line voltages and information current are investigated and organized.

Keywords: Matrix Converter, AC to AC Converter, Carrier based algorithms, PSCAD model, Simulation.

1. Introduction

The late impressive intrigue is appeared in the advancement of AC to AC converters otherwise called "Matrix Converters" for Customizable Speed Drive applications [1-4]. Matrix converters are basically constrained commutated cycloconverters comprising of a matrix of bidirectional switches with the end goal that there is a switch for each conceivable association between the information and yield lines. For a three stage AC to three stage AC matrix converter there are nine bidirectional semiconductor switches. A three stage AC to three stage AC matrix converter is appeared in Fig. 1. While working the Matrix Converter, two fundamental focuses must be recalled. The three or any two mixes of the bidirectional switches in any one yield stage ought not to be shut at a similar moment of time [1-4]. Alluding to Fig. 1, if any two or all of switches SAa, SBa and SCa are shut at the same time, the info lines are short circuited causing unsafe short out streams through the bidirectional switches. Correspondingly with inductive loads all the three bidirectional changes associated with a yield stage ought not be open all the while [1-4]. One switch at any rate in any yield stage must stay shut. Matrix converter straightforwardly changes over the AC input voltage at any offered recurrence to AC yield voltage with self-assertive sufficiency at any unhindered recurrence without the requirement for a dc connect capacitor stockpiling component at the info side. Sinusoidal info and yield streams can be acquired with solidarity control factor for any heap. It has recovery capacity [1-4]. One constraint of the matrix converter is that the greatest yield voltage accessible is restricted to 86.6 % of the info voltage in the direct balance go.

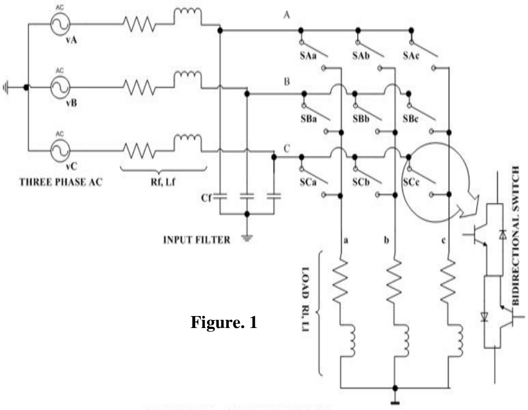

Figure. 1

MATRIX CONVERTER

The genuine advancement of the matrix converter begins with the work of Venturini and Alesina who proposed a numerical examination and presented the Low-Recurrence Adjustment Matrix idea to portray the low recurrence conduct of the matrix converter [5-7]. In this, the yield voltages are acquired by duplication of the tweak matrix or exchange matrix with the info voltages.

The 3 X 3 matrix converter appeared in Fig.1 associates the three stage AC source to the three stage stack. The exchanging Capacity for a 3 X 3 matrix converter can be characterized as takes after:

$$S_{Kj} = \begin{cases} 1 \text{ when } S_{Kj} \text{ is closed} \\ 0 \text{ when } S_{Kj} \text{ is open} \end{cases} \quad (1)$$

$$K \in A, B, C \text{and} j \in a, b, c$$

The above constraint can be expressed in the following form:

$$S_{Aj} + S_{Bj} + S_{Cj} = 1 \qquad (2)$$
$$j \in a, b, c$$

With the above restrictions a 3 X 3 matrix converter has 27 possible switching states [8].
The mathematical expression that represents the operation of a three phase AC to AC Matrix Converter (MC) can be expressed as follows:

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\ S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\ S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t) \end{bmatrix} * \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \qquad (3)$$

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\ S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\ S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t) \end{bmatrix}^T * \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \qquad (4)$$

whereVa, Vb and Vc and iA, iB and iC are the yield voltages and info streams separately. To decide the conduct of the MC at yield frequencies well underneath the exchanging recurrence, a balance obligation cycle can be characterized for each switch. The tweak obligation cycle MKj for the switch SKj in Fig.1 is characterized as in condition 5 beneath:

$$M_{Kj} = \frac{t_{Kj}}{T_S} \qquad (5)$$
$$K \in \{A, B, C\} \text{and} j \in \{a, b, c\}$$

wheret_{Kj} is the on time for the switch S_{Kj}between input phase $K \in \{A, B, C\} \text{and} j \in \{a, b, c\}$ and $T_S$is the time of the PWM exchanging sign or examining period. Regarding the adjustment obligation cycle, equations 2, 3 and 4 can be rewritten as given below:

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} M_{Aa}(t) & M_{Ba}(t) & M_{Ca}(t) \\ M_{Ab}(t) & M_{Bb}(t) & M_{Cb}(t) \\ M_{Ac}(t) & M_{Bc}(t) & M_{Cc}(t) \end{bmatrix} * \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} (6)$$

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} M_{Aa}(t) & M_{Ba}(t) & M_{Ca}(t) \\ M_{Ab}(t) & M_{Bb}(t) & M_{Cb}(t) \\ M_{Ac}(t) & M_{Bc}(t) & M_{Cc}(t) \end{bmatrix}^T * \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} (7)$$

$$M_{Aj} + M_{Bj} + M_{Cj} = 1, \ j \in \{a, b, c\} \quad (8)$$

2. Algorithms for matrix converters

The regulation issue experienced in matrix converters can be communicated as takes after:
Give the information and yield voltages a chance to be communicated as in condition 9 and 10 beneath

$$:v_i = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = V_{im} * \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t + \frac{4\pi}{3}) \\ \cos(\omega_i t + \frac{2\pi}{3}) \end{bmatrix} (9)$$

$$v_0 = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = q * V_{im} * \begin{bmatrix} \cos(\omega_0 t) \\ \cos\left(\omega_0 t + \frac{4\pi}{3}\right) \\ \cos\left(\omega_0 t + \frac{2\pi}{3}\right) \end{bmatrix} (10)$$

Where q is the voltage transfer ratio.

2.1 Venturini and Optimum Venturini Modulation Algorithms

The principal strategy for Venturini is the deduction of the exchange matrix by specifically fathoming conditions 6, 9 and 10 utilizing the imperative in condition 8 [1-2]. Figuring changing circumstances straightforwardly from this exchange matrix is troublesome for practical usage [1-2]. For solidarity input displacement factor an advantageous technique for communicating the tweak work is given underneath:

$$M_{Kj} = \frac{t_{Kj}}{T_s} = \left[\frac{1}{3} + \frac{2v_K . v_j}{3. V_{im}^2}\right] \qquad (11)$$
$$\text{for } K = A, B, C \text{and} j = a, b, c$$

This strategy is of little essentialness as a result of the 50 % voltage proportion constraint [1-2].

Venturini's ideal strategy utilizes normal mode expansion procedure characterized in condition 12 beneath:

$$vo = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = q * V_{im} * \begin{bmatrix} \cos(\omega_o t) - \frac{1}{6} * \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} * \cos(3\omega_i t) \\ \cos\left(\omega_o t + \frac{4\pi}{3}\right) - \frac{1}{6} * \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} * \cos(3\omega_i t) \\ \cos\left(\omega_o t + \frac{2\pi}{3}\right) - \frac{1}{6} * \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} * \cos(3\omega_i t) \end{bmatrix} (12)$$

Utilizing vo characterized as in condition 12, for solidarity input displacement factor, the regulation capacity can be communicated as in condition 13 underneath:

$$M_{Kj} = \frac{t_{Kj}}{T_s} = \left[\frac{1}{3} + \frac{2v_K . v_j}{3. V_{im}^2} + \frac{4q}{9\sqrt{3}} * \sin(\omega_i t + \beta_K) * \sin(3\omega_i t)\right] (13)$$

$$\text{for } K = A, B, C \text{and} j = a, b, c \text{and} \beta_K = 0, \frac{2\pi}{3}, \frac{4\pi}{3} \text{ respectively.}$$

2.2 Sunter-Clare modulation algorithm

The Venturini calculation approach is unsatisfactory for shut circle applications where it is required to ascertain the obligation cycle each examining period to achieve voltage control in which yield recurrence is ceaselessly fluctuating with time [10]. To defeat this issue the approach taken is to gauge the information voltage at each examining period and to decide voltage vector extent and proportion and position straightforwardly [9-11]. A streamlined adaptation of Venturini calculation is characterized as far as the three stage information and yield at each inspecting moment [9-11]. This permits the request voltage proportion, yield voltage greatness and edge to be refreshed at each inspecting period which is a necessity for shut circle control [9-11].

For the constant execution of the proposed balance calculation, it is required to gauge any two of three line to line enter voltages. At that point Vim and ωi.t are figured as give underneath [10-11].

$$V_{im}^2 = \frac{4}{9}.[v_{AB}^2 + v_{BC}^2 + v_{AB}.v_{BC}] \quad (14)$$

$$\omega_i.t = \arctan\left[\frac{V_{BC}}{\sqrt{3}.\left(\frac{2.V_{AB}}{3} + \frac{V_{BC}}{3}\right)}\right] \quad (15)$$

Where v_{AB}, v_{BC} are the input line voltages.
The target output peak voltage and position are calculated as follows:

$$V_{om}^2 = (2/3).[V_a^2 + V_b^2 + V_c^2] \quad (16)$$

$$\omega_O.t = \arctan[(Vb - Vc) / (\sqrt{3}.Va)] \quad (17)$$

Where Va, Vb and Vc are the objective stage yield voltages. In a shut circle framework, for example, a field situated or a vector controlled drive framework, the voltage greatness and edge might be immediate yields of the control circle. At that point the voltage proportion is ascertained as takes after:

$$q = \sqrt{\frac{V_{om}^2}{V_{im}^2}} \quad (18)$$

Where q is the desired voltage ratio and V_{im} is the peak input voltage. The triple harmonic terms are found using the following equations:

$$K_{31} = \frac{2q}{9q_m}.\sin(\omega_i t) * \sin(3\omega_i t) \quad (19)$$

$$K_{32} = \frac{2q}{9q_m}.\sin\left(\omega_i t - \frac{2\pi}{3}\right).\sin(3\omega_i t) \quad (20)$$

$$K_{33} = -\sqrt{V_{om}^2}.\left[\frac{1}{6}.\cos(3\omega_o t) - \frac{1}{4q_m}.\cos(3\omega_i t) \quad (21)\right]$$

Where q_m is the maximum voltage transfer ratio which is 0.866. Then the three modulation functions for output phase a are given as follows.

$$M_{Aa} = \frac{1}{3} + k_{31} + \frac{2}{3V_{im}^2}.(v_a + k_{33}).\left(\frac{2v_{AB}}{3} + \frac{v_{BC}}{3}\right) \quad (22)$$

$$M_{Ba} = \frac{1}{3} + k_{32} + \frac{2}{3V_{im}^2}.(v_a + k_{33}).\left(\frac{v_{BC}}{3} - \frac{v_{AB}}{3}\right) \quad (23)$$

$$M_{Ca} - 1 - (M_{Aa} + M_{Ba}) \quad (24)$$

The adjustment capacities for the other two yield stages b and c are acquired by replacing va with vb and vc in conditions 22 and 23. The tweak capacities have third symphonious segments at the info and yield frequencies added to them to create yield voltage Vo. This is a necessity for getting most extreme conceivable voltage proportion. The three stage yield voltages and information streams can be characterized as far as tweak works as given in conditions 6 to 8.

2.3 Ned Mohan modulation algorithm

A novel bearer based tweak conspire is proposed by Ned Mohan which requires no part data and look-into table to compute obligation proportions, with yield voltage sufficiency 0.866 times that of the info voltage and the information control factor controllable [12-14]. This calculation is quickly clarified beneath: Give the three stage a chance to include voltages, vi = [(vAvBvC)]^T be characterized as in condition 9 and the relating yield stage voltages be characterized as in condition 6 above. The obligation proportions be picked with the end goal that the yield voltages are free of the info recurrence. This is conceivable by considering the information voltages in stationary reference outline and the yield voltages in synchronous reference outline. Henceforth MAa, MBa and MCa are picked as given in condition 25 underneath:

$$M_{Ka} = k_a * \cos(\omega_i t - \varphi_i - \gamma) \quad (25)$$

Utilizing condition 6, 9 and 25 and streamlining, the yield voltage condition va for Stage a diminishes to the accompanying:

$$v_a = \frac{3}{2} * k_a * \cos(\varphi_i) \quad (26)$$

Condition 26 demonstrates that the yield stage voltage va is free of the info recurrence however subordinate just on the adequacy of the information voltage. The adjustment list ka is an element of the yield precise recurrence ω_o as characterized beneath:

$$k_i = k * \cos(\omega_o t - \gamma) \quad (27)$$

Utilizing conditions 26 and 27, the yield stage voltage va disentangles to the accompanying::

$$v_a = \left[\frac{3}{2}.k.V_{im}.\cos(\varphi_i) * \cos(\omega_o t)\right] \quad (28)$$

From condition 25 and 27, plainly the obligation proportion of the switches takes negative esteems. In any case, the prerequisite is that the obligation proportions of the switches must lie in the range 0 to 1. This is made conceivable by adding balanced obligation proportions to the existing obligation proportions. In this way total estimations of obligation proportions are included. The balance obligation proportion is characterized by condition 29 underneath:

$$D_K(t) - |k_a * \cos(\omega_1 t - \varphi_1 - \gamma)| \quad (29)$$

Thus the new duty ratios are defined below:

$$M_{Ka} = D_K(t) + k_a * \cos(\omega_i t - \varphi_i - \gamma) \quad (30)$$

Using equation 29 in 30, in order that the new duty ratio in 30 lies in the range 0 to 1, the following inequality should be satisfied:

$$0 < 2.|k_a| = 2.k < 1 \quad (31)$$

Thus the maximum value of k_a and k can be 0.5. Using this value, the offset duty ratios are chosen as given below:

$$D_K(t) = |0.5 * \cos(\omega_i t - \varphi_i - \gamma)| \quad (32)$$

To utilize the input voltage capability to the full extend, additional common mode voltage term is added which gives the new modulation index as given below:

$$M_{Ka} = D_K(t) + [k_a - \{\max(k_a, k_b, k_c) + \min(k_a, k_b, k_c)\}/2] * \cos(\omega_i.t - \varphi_i - \gamma) \quad (33)$$

In equations 25 to 33, the symbols K, j and γ are defined as follows:

K = A, B, C; j = a,b,c and γ = 0, $\frac{2\pi}{3}, \frac{4\pi}{3}$ respectively.

To calculate input power factor, the input current is represented as a function of duty ratios and output currents, as defined in equation 7 above. Hence the input current in phase A can be expressed as follows:

$$i_A = (k_a.i_a + k_b.i_b + k_c.i_c) * \cos(\omega_i t - \varphi_i) \quad (34)$$

In equation 34, the modulation index and output currents are at output frequency. Equation 34 simplifies to the following:

$$i_A = \left(\frac{3}{2}.k.I_O.\cos(\varphi_O)\right) * \cos(\omega_i t - \varphi_i) \quad (35)$$

Where IO is the abundancy of the yield current and φO is the yield control factor point.

Contrasting condition 35 and the information stage voltage vA, it is seen that the info current slacks the information stage voltage by a point of φ_i. In this way φ_i is been zero for solidarity input control factor operation. Additionally correlation of condition 28 with condition 10 uncovers the accompanying association with q:

$$q = \left[\frac{3}{2}.k * \cos(\varphi_i)\right] \quad (36)$$

3. Model development

To think about the execution of the three stage matrix converter utilizing all the above algorithms, a model was created for each algorithm, utilizing PSCAD [15]. The information utilized for every one of the algorithms are given in Table I.

Table 1: Parameters

Sl.No.	Parameter	Value	Unit
1)	RMS Line to Neutral Input Voltage	220	Volts
2)	Input Frequency	50	Hz
3)	Output Frequency	50	Hz
4)	Modulation Index q / k	0.4 / 0.26667	--
5)	Carrier Switching Frequency	5	kHz
6)	Output RLC Filter	10, 2e-3, 0.50712e-6	Ω, H, F
7)	R-L Load	50, 0.5	Ω, H

In Table 1, the estimation of q and saw-tooth transporter are utilized for Venturini, Ideal Venturini and Sunter-Clare algorithm whereas the estimation of k and triangle bearer are utilized for Ned Mohan algorithm.

4. Simulation results

For the Venturini and the ideal Venturini algorithm, condition 11 and conditions 12 with 13 were utilized to decide the obligation cycle for the nine bidirectional switches, for the previous and the later algorithm separately. For the Sunter-Clare algorithm, conditions 22 to 24 and for the Ned Mohan algorithm condition 33 were utilized to decide the obligation cycle for the nine bidirectional switches. On account of Ned Mohan algorithm, the k esteem was determined for a q were utilized to decide the obligation cycle for the nine bidirectional switches. On account of Ned Mohan algorithm, the k esteem was determined for a q estimation of 0.4 utilizing condition 36 expecting solidarity input control factor [16-17].

The reenactment comes about identifying with Venturini, Ideal Venturini, Sunter-Clare and Ned Mohan algorithm are appeared in Fig.2, 3, 4 and 5 separately. These outcomes are classified in Table II.

5. Discussion of results

From the recreation comes about appeared in Table II, it is seen that the pinnacle principal estimation of line to nonpartisan voltage is most elevated for Ideal Venturini and least for Ned Mohan.

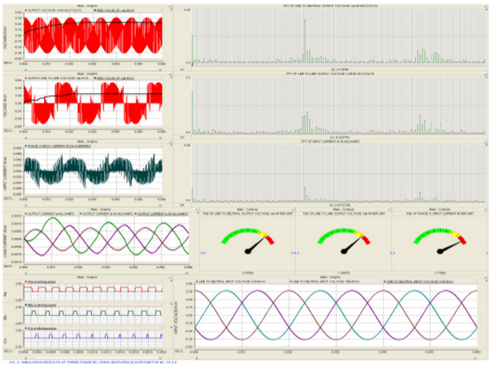

Figure 2: PSCAD Simulation results: Venturini Algorithm

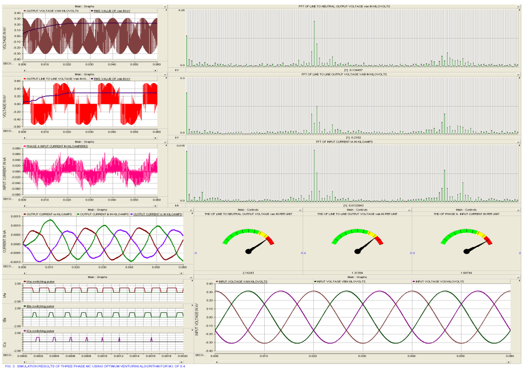

Figure 3: PSCAD Simulation results: Optimum Venturini Algorithm

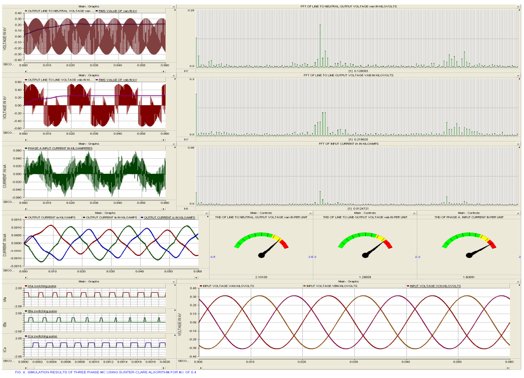

Figure 4: PSCAD Simulation results: Sunter-Clare Algorithm

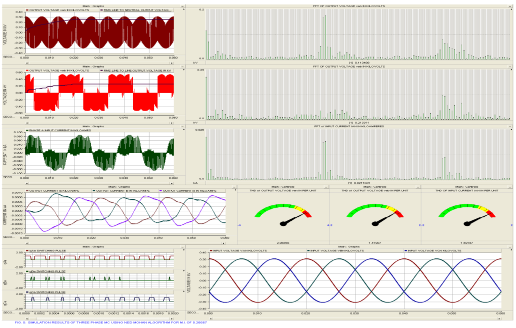

Figure 5: PSCAD Simulation results: Ned Mohan Modulation Algorithm

Table 2: Simulation Results

Sl. No.	Name of Algorithm	Parameters	Peak Fundamental Value			Total Harmonic Distortion		
			Line to Neutral Voltage (V)	Line to Line Voltage (V)	Input Current (A)	Line to Neutral Voltage (p.u.)	Line to Line Voltage (p.u.)	Input Current (p.u.)
1)	Venturini	Table 1	128.38	222.79	13.13	2.183	1.246	1.718
2)	Optimum Venturini	Table 1	134.45	218.2	13.29	2.142	1.313	1.647
3)	Sunter-Clare	Table 1	128.09	218.62	12.47	2.101	1.298	1.608
4)	Ned Mohan	Table 1	113.48	213.31	21.16	2.968	1.419	1.591

algorithm. For Line to Line voltage top essential Sunter-Clare algorithm gives the most astounding quality and Ned Mohan algorithm gives the least esteem. The Information Current pinnacle crucial is most elevated for Ned Mohan algorithm and least for Sunter-Clare algorithm. The THD of line to impartial voltage, line to line voltage and info current all together is the most reduced for Sunter-Clare, Venturini and Ned Mohan algorithm separately. The straight range for balance record for Venturini algorithm is 0 to 0.5 and for Ideal Venturini and Sunter-Clare algorithm this esteem is in the range 0 to 0.866. For Ned Mohan algorithm, the straight adjustment run is from 0 to 0.577. The adjustment list is in the direct range for all the above algorithms and there for the anticipated execution will yield just comparable outcomes as long as the regulation list is inside the straight range. The anticipated execution here has just minor contrasts contrasted with that without yield channel [16].

6. Conclusions

Four transporter based algorithms for exchanging three stage AC to three stage AC Matrix Converter have been considered in detail by demonstrating utilizing PSCAD. The relative benefits of each algorithm from the perspective of high pinnacle central esteem and low THD have been examined and classified. The algorithm number 3 and 4 of Table 2 are as of late proposed. The tweak record is inside the straight range for all the four algorithms and thus the anticipated execution is legitimate for all estimations of balance list inside the direct adjustment run.

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