

OPTIMISED SPACE VECTOR ALGORITHM FOR SEVEN LEVEL CASCADED HYBRID INVERTER USING DECOMPOSITION METHOD

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Abstract: This paper deals with the space vector modulation and its optimization techniques. Previously this work has been done for 5 level cascaded inverters. The main objective of this project is to reduce the total harmonic distortion and switching losses in a multilevel inverter. The model is done by MATLAB/Simulink environment. In this paper the work is tried for seven level cascaded hybrid inverters. The two optimal techniques commonly prevailing for SVM are decomposition method and hexagonal coordinate method. Here decomposition method is discussed in detail. An optimal harmonic profile is obtained when the two middle space vectors are centered in each switching cycle. By this switching losses and THD are reduced. The model is done by MATLAB/ Simulink environment. The strategies have been confirmed by both simulation and experimental results obtained using a cascaded seven level hybrid inverter.

Keywords: PWM, SPWM, SVPWM, Cascade H Bridge, Multi Level Inverter.

1. Introduction

The most important problems in controlling a VSI with variable amplitude and frequency of the output voltage is to obtain an output waveform as much as possible of sinusoidal shape employing simple control techniques. Indeed, current harmonics caused by non sinusoidal voltage feeding imply power losses, electromagnetic interferences (EMI), and pulsating torques in ac motor drives. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy. Under the aspect of harmonic content reduction, multilevel inverters are of the highest

importance. They are particularly suitable in high-power applications when the semiconductor devices are not able to operate at high switching frequencies. The inversion process of converting DC into AC has taken place for many applications such as renewable energy technology, HVDC transmission, Adjustable speed drives and high frequency industrial heating processes. The applications using variable frequency inverters are increasing day by day due to its user friendly approach for common men while the technology behind this is very advance. The aim of this paper is to simulate Space vector pulse width modulation technique with carrier frequency sending for Multilevel Hybrid cascade Inverter.

While many different multilevel converter topologies have been proposed, the two most common topologies are the Cascaded Inverter and its derivatives, and the Diode Clamped inverter. The two most popular control strategies for these multilevel inverter topologies are Carrier and Space Vector (SVM) modulation. Carrier based modulation techniques control each phase leg of the inverter separately and allow the line to line voltage to be developed implicitly.

2. Cascade H Bridge Seven Level Inverter

The cascade H-bridge converters consist of a number of H-bridge power conversion DC Sources, each supplied by an isolated source series-connected on the AC side. In some systems these sources may be available through batteries or photovoltaic cells but in most drive systems transformer/rectifier sources are used for two stage conversion system. Combined in

series, an effective switching state can be related to the switching states of the individual cells.

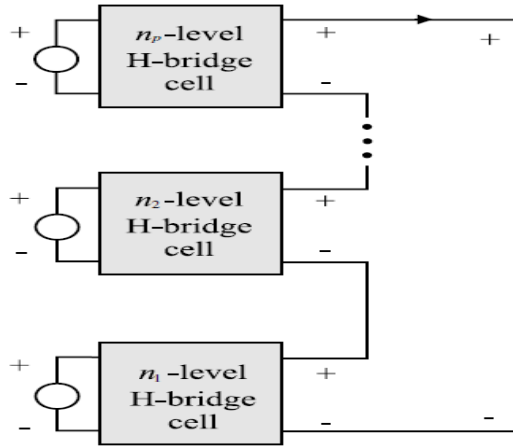


Figure 1. Cascade Multi Level H Bridge Inverter Concepts

For this converter, the effective number of voltage levels is the product of the voltage levels of the individual cells or DC voltage applied to each cell is set to the same value, then the effective number of voltage levels may be related to the number of cells by

$$n = \prod_{i=1}^{i=p} n_i$$

Assuming that the DC voltage of cell i is set based on the adjacent cell. The modulation index for H bridge inverters is:

$$m_H = \frac{\sqrt{2}v_s}{v_{DC}}$$

Where V_s is voltage magnitude of inverter output and V_{dc} is the DC supply voltage to inverter. The value of modulation index varies between ranges:

$$0 \leq m_H \leq \frac{2}{\sqrt{3}}$$

3. Space Vector Modulation

Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently. This technique results in higher magnitude of fundamental output voltage available compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states.

SVPWM method the output voltage is approximated by using the nearest three output vectors that the nodes of the triangle containing the reference vector in the space vector diagram of the inverter. When the reference vector changes from one region to another, it may induce an output vector abrupt change. In addition we need to calculate the switching sequences and switching time of the states at every change of the reference voltage location. Thus the computational complexity is greatly increasing with the increasing number of the reference vectors and it is a main limitation of the application of this typical. In this paper, a new method is proposed in which the even-level inverter is decomposed into six space vector diagrams of four-level inverters. In turn, each of these six space vector diagrams of four-level inverter is decomposed into six space vector diagrams of three-level inverters and each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. Thus the remaining necessary procedures for the seven-level SVPWM are done like conventional two-level inverter. This modification can reduce considerably the computational time and reduce the algorithm complexity. We use the redundancy of certain vectors of the space vector diagram of the inverter in order to ensure the stabilization of the input DC voltages of the inverter.

3.1 Optimized Space Vector Sequences

Figure 2 shows the space vector diagrams for 3 and 5 level Diode Clamped systems, where each digit of the space vector identifier represents the voltage level to which the A, B and C phase legs are respectively switched. Note that some switched states are redundant and create the same space vectors. The difficult task of selecting the optimum set of these space vectors for a given reference phasor was recently solved by Celanovic et al. using a linear coordinate transformate and identified that the harmonic profile of the overall switched waveform is minimized when the nearest three space vectors are used. However, this solution does not identify how to sequence or place these three nearest space vectors in the (half carrier equivalent) switching period so as to minimize the total number of switching transitions and fully optimize the harmonic profile of the output voltage. For a three phase inverter the minimum number of switch transitions in one switching cycle under continuous modulation is 3 (ie. one per phase leg), so that the converter cycles through 4 switched states in each switching period. At least the first and last of these must be a redundant space vector state if only the three nearest space vectors are to be

used (eg. 101 – 201 – 211 – 212).

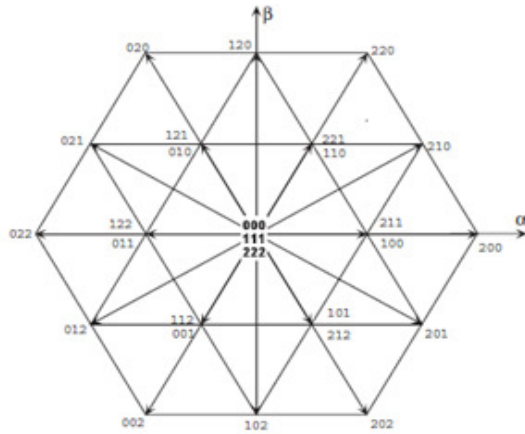


Figure 2(a). Space Vector Status for 3 Level NPC Converter

Depending where in the $\alpha\beta$ space the reference phasor is located, there are two alternatives for this sequence, viz: (i) Select two vectors of even redundancy and one vector of odd redundancy (eg. 211/100, 221/110 and 210), or: (ii) Select one vector of even redundancy and two vectors of odd redundancy (eg. 211/100, 200 and 210). (For two level inverters, only case (ii) is possible since the zero state vector is the only redundant switch combination.) Figure 3 illustrates a subset of a 5 level Space Vector plot, and Table 1 summarizes all possible sequences for this subset that achieve the required minimum of three switching transitions per phase leg in a switching period. Note that from two levels SVM theory it is well known that these sequences should be reversed in the next switching cycle for minimum harmonic impact and so the reverse sequences need not be explicitly considered.

For triangles (b) and (d) there is only one possible sequence. For triangles (a) and (c) the “correct” sequence can be identified from the possible alternatives by ensuring that no extra switching transitions occur when moving between triangles. For example, sequence c(i) should be used when moving from triangle (b) to (c) since it begins with the same state as the sequence in (b), or sequence c(ii) should be used when moving from triangle (c) to (d) since it begins with the same state as the sequence in (d). Within triangle (c) sequences c(i) and c(ii) must be swapped at some point, and this is most conveniently done when the duty cycle for the space vector {431/320} exceeds that of {421/310}.

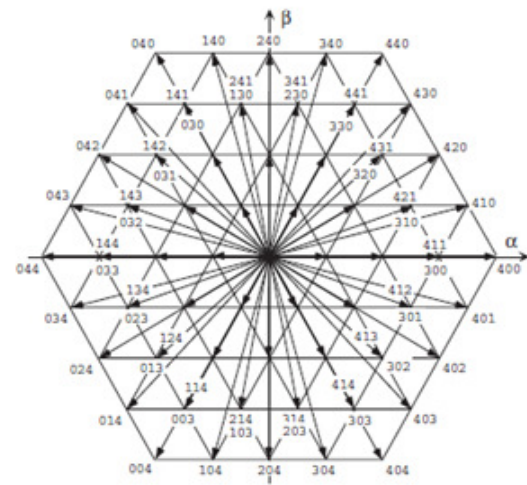


Figure 2(b). Space Vector Status for 5 Level NPC Converter

Applying this principle to triangle (a) means that sequences a(i) and a(ii) cannot be used because they will introduce extra switching transitions when moving into triangle (c).

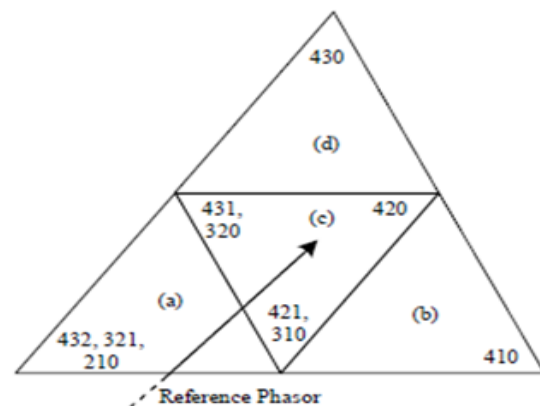


Figure 3. Subset of 5 level Space vector Diagram. In Triangles (a) and (c) 2 vectors of even redundancy and 1 of odd redundancy exist. In Triangles (b) and (d) 1 vector of even redundancy and 2 of odd redundancy exist.

This is very important if the reference phasor lies near the boundary of triangles (a) and (c) because it will cross the linear boundary between triangles (a) and (c) twice in a fundamental cycle, and there are many type (c) triangles in the space vector plot. So only sequences a(iii) and a(iv) can be used, and these are identical to sequences c(i) and c(ii) except that state

{420} has been replaced by state {321}. Hence only state {321} of the triply redundant vector {432/321/210} is useable. Similar analysis for vectors with even redundancies greater than three reveals that only two states can ever be used to achieve minimal switching, and for vectors with odd redundancies greater than two, only one state is useable. Note also that all useful sequences begin and end with an even redundant space vector state. While the above analysis is from the perspective of a Diode Clamped topology the only significant difference with the Cascaded topologies is that there is a greater variety of redundancies. A similar analysis for Cascaded type inverter systems leads to an identical restriction on states and sequences which can be used to achieve the minimum number of switching transitions in a fundamental cycle.

Triangle	Sequence
(a)	(i) {432 to 431 to 421 to 321}
	(ii) {210 to 310 to 320 to 321}
	(iii) {421 to 321 to 320 to 310}
	(iv) {431 to 421 to 321 to 320}
(b)	{421 to 420 to 410 to 310}
(c)	(i) {421 to 420 to 320 to 310}
	(ii) {431 to 421 to 420 to 320}
(d)	{431 to 430 to 420 to 320}

Table 1. Possible Sequences in Five level space vector subset (see Figure 3). Reverse sequences are not shown

4. Basic Principle of Proposed Decomposition Method

The space vector diagram of multilevel inverter can be divided into different forms of sub-diagrams, in such a manner that the space vector modulation becomes more simple and easy to implement, as made in several works. But these works do not reach a generalization of the two-level SVPWM to the case of multilevel inverters; either they divide the diagram into triangles, or into interferred geometrical forms.

The decomposition method is a simple and fast one that divides the space vector diagram of seven-level inverter, within three steps, into several small hexagons, each hexagon being space vector diagram of two-level inverter, as shown in Fig.5-7. Thus the space vector diagram of seven-level inverter becomes very simple and similar to that of conventional two-level

space vector diagram. To reach this simplification, two steps have to be done. Firstly, from the location of a given reference voltage, one hexagon has to be selected among the hexagons. Secondly we translate the origin of the reference voltage vector towards the centre of the selected hexagon.

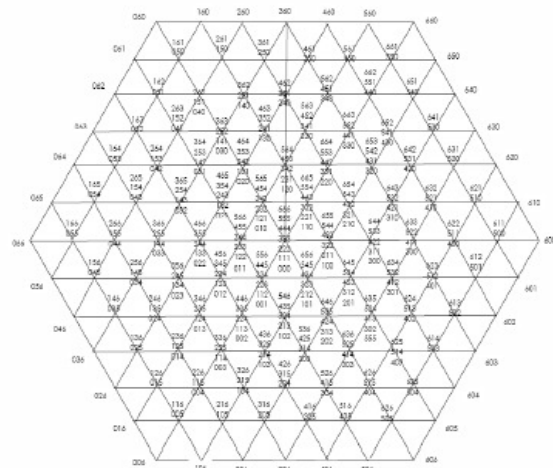


Figure 4. Space vector diagram of seven – level inverter.

4.1 First Correction of Reference Voltage Vector

Having the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that contain the seven-level space vector diagram Fig. 5. There exist some regions that are overlapped by two adjacent small hexagons. These regions will be divided in equality between the two hexagons as shown in Fig. 8. Each hexagon is identified by a number 's' defined as given in Table 2. After selection of one hexagon, we make a translation of the reference vector V_7^* towards the centre of this hexagon, as indicated in Fig. 9. This translation is done by subtracting the centre vector of the selected hexagon from the original reference vector. Table 3. gives the components d and q of the reference voltage V_4^* after translation, for all the six hexagons. The index (3) or (4) or (7) above the components indicate three or four or seven-level cases respectively.

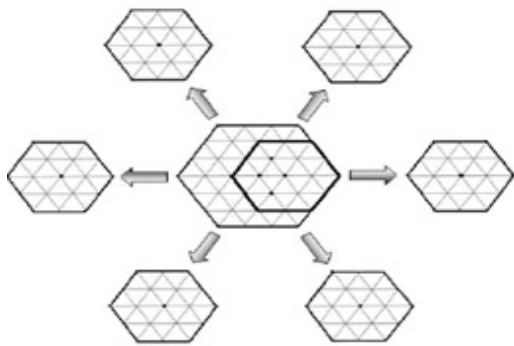


Figure 5. Decomposition of space vector diagram of seven-level inverter into four-level.

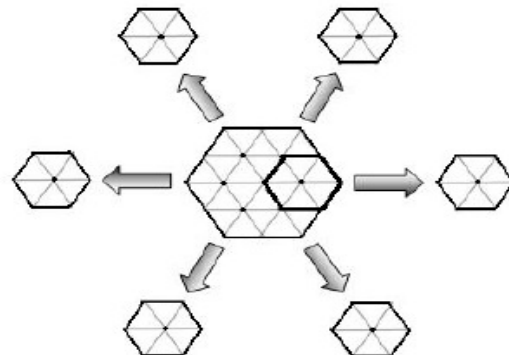


Figure 8. Decomposition of space vector diagram of three-level inverter into two-levels.

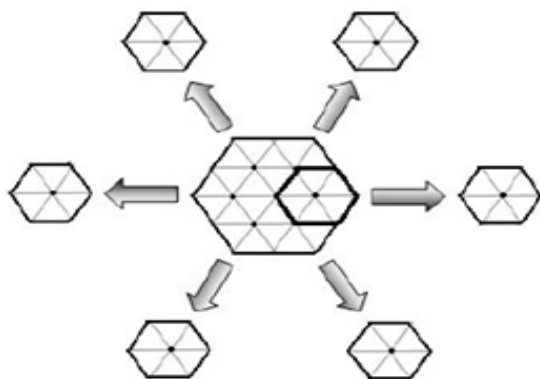


Figure 6. Decomposition of space vector diagram of four-level inverter into three-level.

Table 2. Selection of hexagons based on angle ' θ '

Hexagon 'S'	Location of reference voltage vector phase angle ' θ '
1	$-\pi/6 < \theta < \pi/6$
2	$\pi/6 < \theta < \pi/2$
3	$\pi/2 < \theta < 5\pi/6$
4	$5\pi/6 < \theta < 7\pi/6$
5	$7\pi/6 < \theta < 3\pi/2$
6	$3\pi/2 < \theta < -\pi/6$

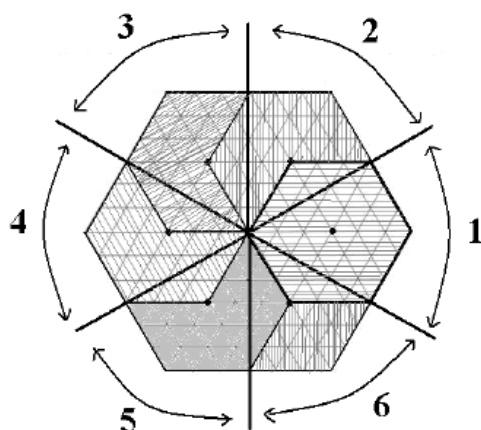


Figure 7. Division of overlapped regions

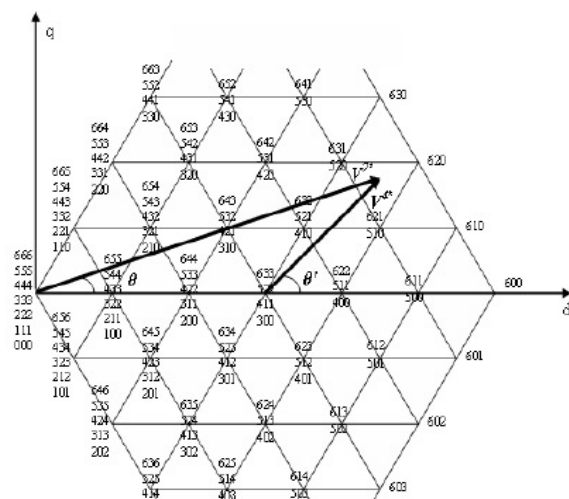


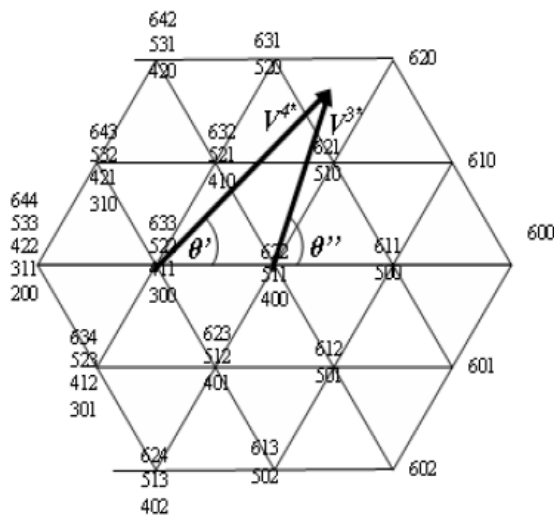
Figure 9. First Translation of Reference Voltage Vector.

Table 3. First Correction of Reference Voltage Vector

S	V_d^{4*}	V_q^{4*}
1	$V_d^{7*} - \frac{1}{2} \cos(0)$	$V_q^{7*} - \frac{1}{2} \sin(0)$
2	$V_d^{7*} - \frac{1}{2} \cos(\pi/3)$	$V_q^{7*} - \frac{1}{2} \sin(\pi/3)$
3	$V_d^{7*} - \frac{1}{2} \cos(2\pi/3)$	$V_q^{7*} - \frac{1}{2} \sin(2\pi/3)$
4	$V_d^{7*} - \frac{1}{2} \cos(\pi)$	$V_q^{7*} - \frac{1}{2} \sin(\pi)$
5	$V_d^{7*} - \frac{1}{2} \cos(4\pi/3)$	$V_q^{7*} - \frac{1}{2} \sin(4\pi/3)$
6	$V_d^{7*} - \frac{1}{2} \cos(5\pi/3)$	$V_q^{7*} - \frac{1}{2} \sin(5\pi/3)$

4.2 Second Correction of Reference Voltage Vector

Having the selected four-level inverter diagram and the location of the translated vector, one hexagon is selected among the six small hexagons that contain this four-level diagram Fig. 6. Here also the overlapped regions are equally divided between the two hexagons. After selection of one hexagon, we make a translation of the reference vector $V4^*$ towards the centre of this hexagon, as indicated in Fig. 10. This translation is done by subtracting the centre vector of the selected hexagon from the original reference vector. Table 4 gives the components d and q of the reference voltage $V3^*$ after translation, for all the six hexagons.

**Figure 10.** Second Translation of Reference Voltage Vector.**Table 4.** Second Correction of reference voltage vector

S	V_d^{3*}	V_q^{3*}
1	$V_d^{4*} - \frac{1}{6} \cos(0)$	$V_q^{4*} - \frac{1}{6} \sin(0)$
2	$V_d^{4*} - \frac{1}{6} \cos(\pi/3)$	$V_q^{4*} - \frac{1}{6} \sin(\pi/3)$
3	$V_d^{4*} - \frac{1}{6} \cos(2\pi/3)$	$V_q^{4*} - \frac{1}{6} \sin(2\pi/3)$
4	$V_d^{4*} - \frac{1}{6} \cos(\pi)$	$V_q^{4*} - \frac{1}{6} \sin(\pi)$
5	$V_d^{4*} - \frac{1}{6} \cos(4\pi/3)$	$V_q^{4*} - \frac{1}{6} \sin(4\pi/3)$
6	$V_d^{4*} - \frac{1}{6} \cos(5\pi/3)$	$V_q^{4*} - \frac{1}{6} \sin(5\pi/3)$

4.3 Third Correction of Reference Voltage Vector

After selection of three-level inverter diagram and the location of the translated vector, one hexagon is selected among the six small hexagons that contain this three-level diagram Fig. 11. Here also the overlapped regions are equally divided between the two hexagons. After selection of one hexagon, we make a translation of the reference vector $V3^*$ towards the center of this hexagon, as indicated in Fig. 9. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table 4. gives the components d and q of the reference voltage $V2^*$ after translation, for all the six hexagons.

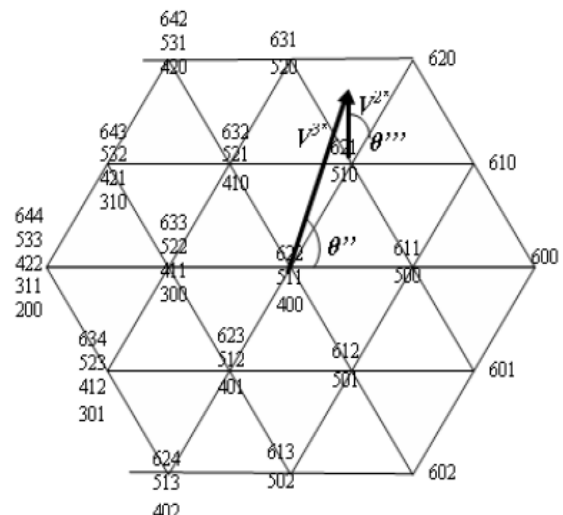
**Figure 11.** Third Translation of Reference Voltage Vector.

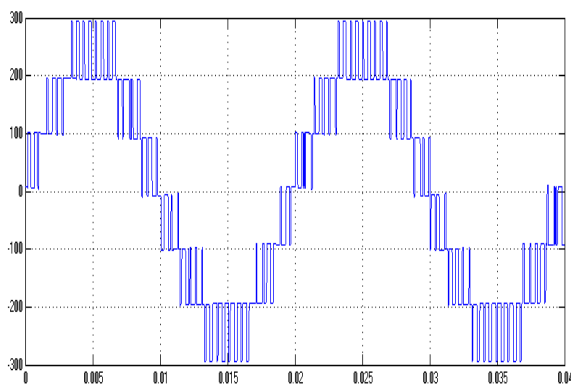
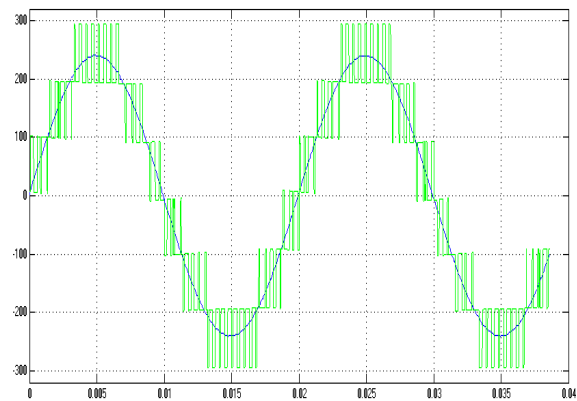
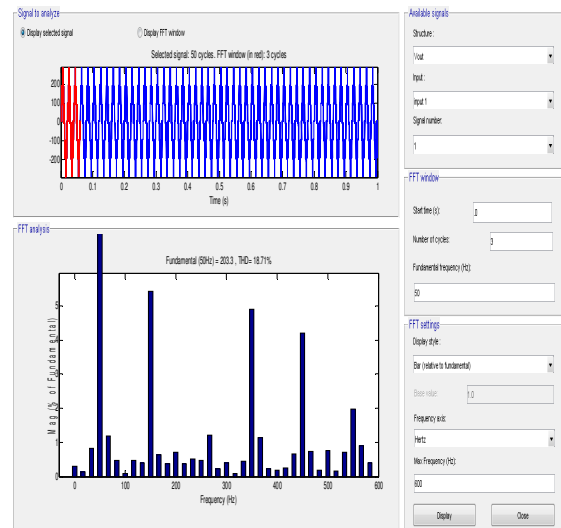
Table 5. Third Correction of reference voltage vector.

S	V_d^{2*}	V_q^{2*}
1	$V_d^{3*} - \frac{1}{6} \cos(0)$	$V_q^{3*} - \frac{1}{6} \sin(0)$
2	$V_d^{3*} - \frac{1}{6} \cos(\pi/3)$	$V_q^{3*} - \frac{1}{6} \sin(\pi/3)$
3	$V_d^{3*} - \frac{1}{6} \cos(2\pi/3)$	$V_q^{3*} - \frac{1}{6} \sin(2\pi/3)$
4	$V_d^{3*} - \frac{1}{6} \cos(\pi)$	$V_q^{3*} - \frac{1}{6} \sin(\pi)$
5	$V_d^{3*} - \frac{1}{6} \cos(4\pi/3)$	$V_q^{3*} - \frac{1}{6} \sin(4\pi/3)$
6	$V_d^{3*} - \frac{1}{6} \cos(5\pi/3)$	$V_q^{3*} - \frac{1}{6} \sin(5\pi/3)$

space vector diagram is further decomposed into six two level space vector diagrams and the switching states of seven level space vector diagram are changed in to its equivalent two-level switching states. The optimum sequence of these three states is selected so as to minimize the total number of switching transitions and fully optimize the harmonic profile of the output voltage. Note that from two level space vector modulation theory, it is well known that these sequences should be reversed in the next switching interval for minimum harmonic impact.

5. Simulation using Simulink

In order to prove the validity of the proposed space vector pulse width modulation (SVPWM) using decomposition method, a three phase seven-level inverter fed the load is simulated with the simulation parameters. The simulation results of seven-level inverter are shown in Fig. 12- 14.

**Figure 12.** Simulated result of output voltage.**Figure 13.** Simulated Result of output voltage compared with carrier waveform.**Figure 14.** THD Results by FFT analysis.

6. Conclusion

In this paper, space vector pulse width modulation using decomposition method has been proposed and described for a seven-level inverter. Thus the proposed method reduces the algorithm complexity and the execution time. It can be applied to the multi-level inverters above the seven-level also. The obtained total harmonic distortion (THD) with the proposed method for seven-level is improved 3.3% from the other conventional methods of SVPWM techniques. The THD is very less as compared with the other conventional methods of SVPWM techniques. The paper also presented a salient feature of SVPWM. This

paper will serve as a valuable resource to any future worker in this important area of research. This project can further be extended to nine level or more for minimum THD results and minimum switching losses.

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