Implementation of OFDM System using FPGA

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Abstract

OFDM provides high bandwidth competence since the carriers are orthogonal to each other and multiple carriers allocate the data among themselves. The main benefit of this transmission technique is their sturdiness to channel fading in wireless communication environment. The OFDM is the largest utilized recently, principally, because of it use the efficient FFT to do the modulation. This work describes how to implement an OFDM modem on FPGA using VHDL for a 31 subcarrier (channels) OFDM system using 64 points radix-4 FFT time decimation, a CORDIC implementation to execute the butterfly calculus, and each channel modulation will use a 4-QAM constellation. The system is divided in a transmission section and a reception section. The main purpose of this task is to implement & test an OFDM transmitter and receiver using a FPGA.

Key Words: FPGA, OFDM, QAM, FFT.

Introduction

The OFDM technique (Orthogonal Frequency Division Multiplexing) has been worn in the last years in applications that require a huge transmission rate like ADSL modem, wireless network (Wi-Fi 802.11), DVB (Digital Video Broadcasting) and DAB (Digital Audio Broadcasting). In all these cases, one needs to implement an integrated circuit (IC) that performs the necessary chip functions. For prototyping circuits FPGA is better choice than using ASIC (Application Specific Integrated Circuit), CUSTOM or SEMICUSTOM. FPGA implementations because avoid the:

1. Initial costs.
2. Great development time and the inherent risks of conventional ASIC.

So, in this way, the development of high advanced techniques of digital data transmission and the actual FPGA stage of integration make possible the building all the circuits that compounds a digital communication systems in an unique chip.

To make use of this recent technologies of data transmission, it is necessary the development efficient techniques of digital modulation. The OFDM is the biggest utilized recently, principally, because of it use the efficient FFT to do the modulation. This work describes how to implement an OFDM modem on FPGA using VHDL for a 31 subcarrier (channels)

OFDM system using 64 points radix-4 FFT time decimation, a CORDIC implementation to perform the butterfly calculus, and each channel modulation will use a 4-QAM constellation. The system is divided in a transmission section and a reception section.

1 OFDM Transmitter

The form considered for the achievement of the OFDM transmitter is the shown in the Fig.1, and basically consist of the following blocks:

1. Serial to parallel converter.
2. Constellation modulator.
3. The IFFT block.
4. Parallel to serial converter.
5. Digital to Analog converter.

Figure 1: OFDM Transmitter.

The serial to parallel converter collect the M series of bits to be transmitted, and those bits are separated into N sub blocks of mn bits of each sub block. Individuals N sub blocks will be mapped by the
gathering modulator using Gray codification, this means \( an + jbn \) values are obtained in the gathering of the modulator.

The M-QAM encoder converts i/p data into composite valued gathering points, according to a certain constellation, 4-QAM, 16-QAM, 32-QAM & so on. The quantity of data transmitted on apiece subcarrier depends on the constellation, of 4-QAM & 16-QAM transmit two & four data bits per subcarrier, respectively. Which constellation to employ depends on the quality of the communications channel. In a channel with towering interference a small modulation scheme like BPSK is encouraging, since the required signal to noise ratio in the receiver is low, whereas in a hindrance free channel a superior constellation is more favorable due to the higher bit rate. It is necessary to identify how the constellation will be mapped to execute that block. However, separately from layout of the gathering, the block encoder can be made through consulting a conversion table, implemented by means of a LUT (Look Up Table) that exists in LCs (Logic Cells) of FPGAs. It is important to observe that in that mapping block, bits are renewed into complex symbols (phasors) having the in sequence of the constellation into its I, Q components.

The Inverse Fast Fourier Transform transforms the signals as of the frequency domain to the time domain, an IFFT converts a amount of complex data points, of extent that is power of 2, into the different numeral of points but in the time domain. The numeral of subcarriers determines how various subbands the accessible spectrum is split into the cyclic prefix is a replica of the last \( N \) samples from the IFFT, which are sited at the commencement of the OFDM frame. There are two reasons to interleave a cyclic prefix. Pretentious that the cyclic prefix is longer than the channels impulse response, the convolution among the data and the channel impulse response will perform like a circular convolution and intervention from the preceding sign will only involve the cyclic prefix. The cyclic prefix is then redundant within the receiver and the circular convolution makes equalization in the receiver easier. Nonetheless, if the number of samples in the cyclic prefix is large, the data transmission rate will diminish significantly, while the cyclic prefix does not carry any useful data. Thus, it is essential to choose the minimum necessary cyclic prefix to maximize the efficiency of the system [1] [2] [3] [5].

### 2 OFDM Receiver

The blocks of the OFDM receiver are shown in the Figure 2.

1. Analog to digital converter.
2. Serial to parallel converter.
3. Cyclic prefix removal.
4. The FFT block.
5. M-QAM decoder.
6. Parallel to serial converter.

#### Figure 2: OFDM Receiver

The received symbol is in time domain and it can be vague due to the effect of the channel. The received signal go through a serial to parallel converter & cyclic prefix removal.

After the cyclic prefix elimination, the signals are passed during an \( N \) point fast Fourier transform to change the signal to frequency domain. The output of the FFT is produced from the former \( M \) samples of the output.

The demodulation can be refined by DFT, or improved, by FFT, that is it capable realization that can be used reducing the process time & hardware. FFT calculates DFT with a great decline in the quantity of operations, leaving several current redundancies in the direct estimate of DFT [4].

At the decoder, a mapped symbol (point) of the transmitted gathering may have changed due to the additive noise in the communications channel, a misadjustment in the sample time at the receiver, or several other unwanted causes. Consequently, it is necessary to define a verge to facilitate the decision making in the receiver constellation. That is the function of the M-QAM decoder.

### 3 Implemented Through Cordic

#### Figure 3: Implemented through CORDIC
1. **Serial to Parallel Conversion**

In Serial to parallel converter data elements are converted from serial data streams to parallel data streams and data elements received in time sequence, that is one at a time, into a data stream consisting of various data elements transmitted simultaneously.

2. **Encoder**

Encoder is a circuit which converts the analog signal to digital signal. Its input is in analog form and output is in digital form.

3. **Dual Port RAM**

Dual port RAM can read and write dissimilar memory cells simultaneously at different addresses. This is the main difference between dual port RAM and single port. RAM, as single port RAM can merely be accessed at one address at a time. Consequently, single port RAM allows merely one memory cell to be read/write during each clock cycle. Moreover, single port RAM uses a six transistor basic ram cell, whereas a dual port ram cell uses an eight transistor cell for memory. This means that the region of a single port RAM cell is smaller than the region of a dual port RAM cell.

4. **Divider Limiter**

The number of carriers in an OFDM system is not only but also restricted by the divider cascade frames; add frame guards, header and trailer.

5. **Multiplier**

Efficient multiplication technique to reduce the partial used for Orthogonal Frequency Division Multiplexing product which is happened in predictable multiplication procedure therefore the FFT and inverse fast Fourier transform (IFFT) with OFDM) modulator & demodulator.

6. **Twiddle Factor**

It is a key component in IFFT/FFT valuation for current orthogonal frequency division multiplexing based treless & wireline communication systems, such as IEEE 802.11a/g, 802.16, DVB, DAB systems.

7. **Hermitian Symmetry**

Hermitian symmetry is used as you want the IFFT output to be real valued, so that it could be transmitted directly over a wire.

8. **Decoder**

It is a circuit which converts the digital signal to analog signal. Its input is in digital form and output is in analog form.

4. **Results and Analysis**

4.1. Simulation Results of Transmitter Section.

In the block diagram of CORDIC, various blocks are included, all these blocks are connected as follows, 4 bit binary input is given to Quadrature Amplitude Modulation (QAM) block. Real and Imaginary components of QAM is specified to Symbol generator block. Output of Symbol generator is given to two Zero padding blocks, one for real and other for imaginary. Output of Zero padding blocks is given to two IFFT blocks. Output of IFFT is given to CP block. Output of CP is given to output module. Output module is a 16 bit binary data and it is transmitter output which is shown in figure 4.

4.2. Simulation Results of Receiver Section.

In the block diagram of CORDIC, all the blocks are connected as follows, OFDM Transmitter output is given to Inverse Cyclic prefix block. Output of Inverse Cyclic prefix block is set to Fast Fourier Transform (FFT) block. Output of FFT is given to Inverse Zero padding blocks. Output of Inverse Zero padding blocks is set to Inverse Symbol generator. Output of inverse symbol generator is set to de-mapping block. Original input data is recovered at de-mapping block.

4.3. Simulation Results of OFDM System.
Figure 6 shows simulation of OFDM system.

Figure 6 shows the result of OFDM transmitter section and OFDM receiver section.

5 Synthesis by using different devices such as Spartan 2, Virtex, Virtex 5.

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Modulation</th>
<th>Spartan 2</th>
<th>Virtex</th>
<th>Virtex-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4 QAM</td>
<td>12.85 nsec.</td>
<td>11.774 ns</td>
<td>2.767 ns</td>
</tr>
</tbody>
</table>

Table 1: Comparison between devices such as Spartan 2, Virtex, Virtex 5.

Table 1 shows the results of synthesis by using different devices such as Spartan-2, Virtex, and Virtex-5. Experimental results are obtained by using different devices. But by using Virtex-5 we are requiring less time to execute the program as compared to other devices such as Spartan-2 & Virtex.

6 Conclusion

OFDM is usually used air interface technology for broadband wireless systems. Due to the inherent nature of the technology, OFDM signals an exhibit hardware requirement that challenges the designers. The different hardware requirements including processing speed, flexibility, time to market necessitate an FPGA based implementation platform. Present work, supplies a code in complete and practical VHDL for a modem OFDM with 31 subcarrier, using a 64-points FFT, radix-4 with CORDIC, at a rate of 12.5 Mbps. Implementation of OFDM system and FPGA synthesis results of all of the major blocks in the OFDM system is verified and experimented by using device Virtex-5 we are requiring less time to execute the program as compared to other devices such as Spartan-2 & Virtex.

References


