An Improved Comparator Structure For 8-Bit SAR ADCs: A Review

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Abstract: Among the popular ADC structures, The Successive Approximation Analog to Digital converters (SAR ADCs) is the widely used structure in many applications for its low power utilization, moderate speed and resolution. The SAR ADC architecture includes sample and hold circuit, successive Approximation Register, digital-to-analog converter and an analog voltage comparator. This paper reviews the conventional SAR ADC designed with conventional comparator and the proposed SAR ADC designed with Efficient Double Tail Dynamic latch Comparator and their performances are compared on power parameters.

Keywords : Analog-to-digital conversion, SAR ADCs, Dynamic Comparator

I. INTRODUCTION

Successive approximation register (SAR) analog-to-digital converters (ADCs) fills the majority of the ADC market for medium- to high-resolution ADCs. SAR ADCs afford up to 5Msps sampling rates with resolutions from 8 to 18 bits. The SAR architecture contributes high-performance, low power ADCs to be packaged in small form factors for today’s demanding applications. For instance, Low power ADCs with moderate resolution and low sampling frequency is suited for biomedical application. These specifications make SAR ADC the suitable choice. It consumes low power due to its simple structure. Moreover The scalable characteristic of SAR ADC with the technology scaling is a boon since most parts of the architecture apart from the comparator are digital. For example, The life time of the artificial pacemakers ought to last up to 10 years which command low power utilization per operation[1] . The analog to digital converter is the critical part of an implantable pacemaker since it expends a lot of force as the interface between sensed analog signal and digital signal processor block. In this manner, diminishing the power utilization of the ADC is a noteworthy concern. ADCs are selected according to specific application within the consideration of resolution, power, size, sampling frequency, performance and etc. For some applications, almost all the architectures may work well, for others, there may be a better choice to achieve the best performance. For example, a Flash ADC is most popular for applications requiring ultrahigh speed when power consumption is not primary concern; A Sigma-Delta ADC is always the best choice when high resolution is demanded; A SAR ADC is always first considered for low power and small size with medium resolution applications[2],[3]. The basic block diagram of SAR ADC is shown in Figure1 .The block includes sample and hold circuit, successive approximation register, digital-to-analog converter and an analog voltage comparator.

The successive approximation register is begun with the most significant bit (MSB) is equal to a digital 1. This code is sent into the DAC, which then supplies the analog equivalent of this digital code (\(V_{ref}/2\)) into the comparator circuit for comparison with the input sampled voltage. If this analog voltage exceeds \(V_{in}\) the SAR resets this bit; otherwise, the bit is left as 1.

Figure 1: Basic SAR ADC Block

Then the next bit is set to 1 and the same process is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital code of the sampled input voltage and is finally drawn as output from the SAR at the end of the conversion (EOC).

This Paper reviews the Conventional SAR ADC and Proposed ADC and comparison of performance parameters of two ADCs. The paper is organized as follows. The conventional and Proposed SAR ADC with its performance parameters are reviewed in section II. section III and IV drives to the conclusion and future scope.

II. LITERATURE REVIEW
The section II-A reviews the conventional SAR ADC designed with the conventional comparator and section II-B reviews with the proposed comparator designed with double tail dynamic latch comparator. Section II-C reviews with the parameters which enrich the performance of ADC.

A. Conventional SAR ADC Structure

![Figure 2: Conventional SAR ADC](image1)

In conventional SAR ADC as shown in figure 2, the main part of the circuit is the 8-bit Successive approximation register, whose output is given to an 8-bit DAC. The analog output of the D/A converter is then compared to an analog signal $V_{in}$ by the comparator. The output of the comparator is a serial data input to the SAR. Till the digital output (8 bits) of the SAR is equivalent to the analog input $V_{in}$, the SAR adjusts itself. The 8-bit latch at the end of conversation holds onto the resultant digital data output. The detailed working is as follows. At the start of a conversion cycle, the SAR is reset by making the start signal high. The MSB of the SAR (b7) is set as soon as the first transition from LOW to HIGH is introduced. The output is given to the D/A converter which is constructed by R-2R ladder structure, produces an analog equivalent of the MSB and is compared with the analog input $V_{in}$ of the conventional comparator. If comparator output is LOW, D/A output will be greater than $V_{in}$ and the MSB will be cleared by the SAR. If comparator output is HIGH, D/A output will be less than $V_{in}$ and the MSB will be set to the next position (b7 to b6) by the SAR. According to the comparator output, the SAR will either keep or reset the b6 bit. This process goes on until all the bits are tried. After b0 is tried, the SAR makes the conversion complete with the valid data on parallel output lines which in turn enables the latch, and digital data appear at the output of the latch. As the SAR determines each bit, digital data is also available serially.

B. Proposed SAR ADC Structure

![Figure 3: Proposed SAR ADC](image2)

In Proposed SAR ADC structure as shown in figure 3, the conventional comparator structure which is highlighted by a rectangular box is replaced by a double tail dynamic latch comparator which is shown below in figure 4, in order to improve its speed and accuracy. The main idea of the proposed comparator is to increase $V_{fn}/f_p$ in order to increase the latch regeneration speed in turn increases the speed of computation as well as enhance the accuracy of the computation.
C. Performance Metrics of ADCs

a. Resolution
The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The resolution determines the magnitude of the quantization error and therefore determines the maximum possible average signal to noise ratio for an ideal ADC without the use of oversampling. The values are usually stored electronically in binary form, so the resolution is usually expressed in "levels", is assumed to be a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since 2^8 = 256. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from −128 to 127 (i.e. signed integer), depending on the application.

b. Differential Nonlinearity
Deviation of the code transition width from the ideal one (1 LSB) is called differential nonlinearity (DNL). For narrow code width, DNL is negative while for the wide one DNL is positive. In an ideal ADC the code width is always one, thus, DNL is zero.

c. Integral Nonlinearity
Integral nonlinearity (INL) is the difference between the code centers from the ideal line. INL can also be specified as the sum of DNLs [4]. Additionally, INL can be defined as the distance of the code centers with the best fit line. Figure 2.4 depicts the maximum INL which is measured with the ideal one.

d. Signal-to-Noise-and-Distortion Ratio
Signal-to-Noise-and-Distortion Ratio (SINAD) is the value of the input signal over the sum of the total noise and harmonic components. Equation indicates the SINAD mathematically
\[
\text{SINAD} = 20\log_{10} \frac{V_{\text{signal}}}{V_{\text{total\ noise+harmonic}}}
\]

e. Effective Number of Bits
Effective Number of Bits (ENOB) is obtained from SINAD. ENOB is commonly used instead of SINAD, since it presents SINAD in the number of bits. ENOB is achieved using Equation
\[
\text{ENOB} = (\text{SINAD}-1.76) \text{dB/6.02 dB}
\]

f. Power Consumption
The total power consumption of a CMOS circuit can be expressed by three terms dynamic power consumption, leakage power consumption and direct path consumption [5]. The last two items are neglected due to their low contribution to the power. The dominant factor is the dynamic power based on the equation:
\[
P = CV^2
\]

g. Figure of Merit
The figure of merit (FOM) used in [6] is referred here to compare the proposed ADC design with other published works. In stead of a power point of view, this FOM is from the aspect of energy, which concerns the total energy consumed in one full conversion cycle of ADC [7]. Figure of Merit is defined as
\[
\text{FOM} = \frac{\text{power}}{2^{\text{ENOB}} \cdot F_s}
\]

III. CONCLUSION

Among the two critical components such as Comparator and DAC in SAR ADC, The speed of the ADC is limited by Comparator since it must resolve small differences in \(V_{in}\) and \(V_{ref}\) of dac within specified time. So the proposed SAR ADC utilizing the double tail dynamic latch comparator which is a low power consumer correspondingly reduce the power consumption of SAR ADC thereby making it more efficient for Biomedical applications than the conventional one.

IV. FUTURE WORK

Since Designing Comparator is the crucial part of the ADC Design, which acts as main part of computation. An efficient comparator is to designed, here double tail dynamic latch comparator have been designed in such a way to increase the performance of the ADC. In future, more parameter analysis can be made and comparisons of different parameters are done and the designs can be further improved to overcome the drawbacks of this structure.

REFERENCES
