Analysis of Submicron Adder Circuits

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Abstract

With the revolution in integrated circuits, great emphasis was given on performance and miniaturization. Speed, area and power became the main criterion upon which a VLSI system is measured in terms of its efficiency. In any VLSI system, a full adder is widely component, which also decides the performance criteria of the system. The analysis and design of Modified Carry Select Adder (MCSLA) is analysed. Basically the adder circuit is designed to achieve low power and less delay and by logic gate of the circuit improves the performances. For speed process high logic circuit is implemented and also to have less propagation. In hybrid CMOS design style various adder cells and transistor is used, but in proposed circuit Dual Rail Signal System (DRPTL) is implemented with the load condition and the clock signal to manage the power flow in the circuit and the process is performed in an efficient way in terms of its gate count and thereby on power and speed.

Index Terms: Carry select adder, dual rail signal system, ripple carry-adder.
1. Introduction

In the past years, many digital applications are designed for scaling down the area of circuitry. Nowadays all the applications like cellphone, laptop have reduced in size tremendously. It is always desirable to reduce area, power and delay for any submicron circuits[1]. Adder circuits are the fundamental element present in most of the digital circuitry. It is used in most of the DSP and microprocessor circuits. Addition is the fundamental operation to perform most of other useful operations like subtraction, multiplication, division, address calculation etc. Adder circuit which is a part of the critical path has vital role is deciding the efficiency of the system.

The total Power dissipation in a CMOS circuit is given as:

\[ P_{\text{total}} = P_{\text{switching}} + P_{\text{static}} + P_{\text{shortcircuit}} \]  

Taking into consideration the Static Power dissipation, let us consider a simple CMOS inverter. In ideal cases, when input to the gate terminal is 0, the NMOS is off and PMOS is on and vice versa. So ideally no leakage current in this operation. But there can be leakage current during this operation, which is a leakage between diffusion region and substrate region of MOS, as per the parasitic diode model. So this leakage current constitute the static power dissipation and is given by:

\[ P_{\text{Static}} = V_{DD} \cdot I_{\text{Leakage}} \]  

The Dynamic power dissipation occurs during switching. While switching either from 1 to 0 or from 0 to 1, for a short duration, both NMOS and PMOS are on. At that time a small short circuit current(I_{SC}) flows from V_{DD} to Ground and the dynamic power dissipation occurs.

\[ P_{\text{ShortCircuit}} = V_{DD} \cdot I_{SC} \]  

\[ P_{\text{Switching}} = \sum_{i=0}^{N} \alpha_i C_i V_{DD} V_{\text{Swing}} f_{\text{clk}} \]  

Figure 1: Switching and Short-Circuit Current Elements in Static CMOS
where $\alpha$ is the switching activity at node $i$.

Propagation delay is how quickly the circuit responds to the change in input and is given by:

$$T_d\alpha = \frac{C_L V_{DD}}{k(V_{DD} - V_{th})^\alpha}$$  \hspace{1cm} (5)

Where, $\alpha$ refer the velocity index saturation.

In well-engineered deep submicron CMOS technologies, the difficult criteria are concentrating on emerging communication process high speed with low power in digital signal processing chip. In the process of arithmetic division, the multipliers and adder are used widely in VLSI system [2]. Since last decades, the growth of the application in electronics is high and it’s major in semiconductor industry. However, reduction of power consumption, delay and area are the critical fear in the logic circuits of any application. [2] The explosive growth and the demands are high in convenient electronic product, high speed, battery life’s, area and the reliabilities of the circuits. [3] In various logic circuits and algorithm like parity checker, converter of code, compressors and error correcting code or detector are basically used the building blocks of XOR-XNOR circuit.

The VLSI circuit power consumption is specified as static power, dynamic power and short circuit power. If the transistors of CMOS (NMOS and PMOS) are active for short duration at a time, then this dissipation of power is short circuit power. As well as the static power will be various the technology of process. But dynamic power depends on load capacitance charging and discharging. The dominant dynamic power is given as

$$\text{Dynamic Power} = \alpha (V_{DD})^2 f C_L$$  \hspace{1cm} (6)

Where, $\alpha$ denotes the activities of switching, voltage supply as $V_{DD}$ and frequency of switching the load capacitance as $f$.

The rest of this article is organized as follows. Section II details the related work with respect to the existing adder circuits. Section III describes the modified circuits with respect to the different adder topologies. Section IV demonstrates the performance analysis of submicron adder topologies and in section V we draw the conclusions.

2. Related Work

For high performances of the execution cores in the logic and arithmetic logic unit the efficiency of energy is essential. For highest power density of the processor block is a part of the adder. It creates a thermal hot spots and sharp temperature gradients to operate the system with the circuit which have high performance. The multiple ALUs presence in modern superscalar processors
and execution cores of chip further associate with aggravates the problem by impacting circuit reliability. [4] It increases the cooling costs for the purposes of design.

At the same time, it critical the performances of the wide adders under different regions and appear of ALUs inside and microprocessor data path of FPUs. Ripple Carry Adder have cascaded “N” single bit full adder and output carry of previous adder as input to next full adder carry. The value of N increases the adder delay in a linear way [5,6]. Therefore, the adder has a lowest speed of RCA with large propagation delay but least are only occupies in it. BEC uses less logic gates than the structure of N-bit full adder.

In real time application, adder circuit is a major part in various logic circuits. Normally, the circuit design is design for consumption of low power to enhance the performance and to address the parameter at chip level. The design of the circuit provides an efficient power delay product (PDP), less propagation delay and low power and area. Therefore, for various design style of logic circuit is built with required performances. When compare the conventional static CMOS logic styles Adder like TGA, TFA, etc the hybrid CMOS design provides a better performance. It achieves a good drivability, delay, power, PDP, energy and noise robustness than the existing circuit.

The essential components are used to design the sophisticated hardware circuits and multiplexer is performed based the topology of pass transistor full adder with less area and transistor count. [7] As well as the CMOS adder circuit is designed based on Tanner EDA using T-SPICE and define the design of the gate 3T-XOR with its significant process. [2] The performances of the arithmetic and logic circuit of adder are illustrated the system performances as per the gate function. In digital systems, if adder lies on the critical path, then the delay of the overall system will increase. In circuit implementation the function of sum and carry is carried out by Pass transistor logic and Gate Diffusion Technique (GDI) respectively. [8, 9] Both functions separate the count of transistor equally.

3. DRPTL and MCSLA Adder

In this logic, Pass-Transistor is processed with the design of low power circuit. In pass network transistor is generated according to its function and perform sum and carry function as per the signal of a clock. At the end of generating voltage swing of the logic is performed. This logic provides improvement in speed, eliminating short circuit current in the output of inverter and includes voltage level restoration. [10-12] The DRPTL logic leads to have an efficient implementation with a clock signal for efficient dynamic access. It provides fast process and dynamic synthesis of logic functions in transistor network.

The process of dual rail signal and single rail system is shown in Fig.2. The proposed logic improves the dynamic circuit speed with the evaluation of clock
signal logic with transistor. The supply of voltage is varied based on the charges phases. If the clock signal is equal to 1 in the evaluation phase, then the circuit will be discharged or pre-charge and if equal to 0 in pre-charge phase, then the circuit is charged and applies to voltage supply level from the transistor.

Normally the power density and dissipation are the main objective and rapid growth in portable systems. In VLSI design, the widely used adder component provides better performances in the integrated circuit. The analysis and design of Carry Select adder (CSLA) is proposed with Modified AOI in a cadence 45nm CMOS. It reduces the delay process with efficient access of better performances. It processes in parallel prefix with sum and carry generating for the high and fast process of circuit. The modified CSLA circuit observed less power consumption and area than the existing circuit with less gate count. By the proposed circuit the gate-level are performed in a simple and easy manner. Based on modification of CSLA bits the process of the circuit is performed in an efficient manner in terms of gate count, power and delay.

The CSLA circuit is modified by replacing cin=1 blocks by modified AOI and thereby the number of gate count is reduced. The gates are replaced by the MUX equivalent circuits as shown in Fig 3. Each AND gate is replaced by the MUX equivalent of it and also applying De Morgans law, the gate count reduces in each group. Therefore, area reduces and thereby reduce the power and delay of the circuit.

Figure 2: (a) Single Rail Signal System, (b) Dual Rail Signal System

Figure 3: Proposed Hybrid Full Adder Topology
4. Performance Analysis

The performance of different adder circuits are compared and studied in these result analysis are studied in Fig.4 and Table I. The performance analysis shows that the modified submicron adders shows better performance compared to the existing ones. The analysis was performed on the basis of VLSI requirement - Power, area and delay of the circuit.

Figure 4: Simulation of Proposed Circuit - Sum Function

Figure 5: Simulation of Proposed Circuit - Carry Function
Figure 6: Proposed Hybrid Full Adder Topology - Sum

Table I: Performance Analysis of Improved DRPTL Adder Circuit

<table>
<thead>
<tr>
<th>Parameters</th>
<th>XOR-XOR</th>
<th>XNOR-XNOR</th>
<th>Centralized</th>
<th>SRPTL</th>
<th>Improved DRPTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. Transistors</td>
<td>24</td>
<td>24</td>
<td>24</td>
<td>19</td>
<td>17</td>
</tr>
<tr>
<td>Power</td>
<td>0.588mW</td>
<td>0.788μW</td>
<td>84.257μW</td>
<td>3nW</td>
<td>2.5nW</td>
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<tr>
<td>Delay</td>
<td>3000ps</td>
<td>3000ps</td>
<td>3000ps</td>
<td>2000ps</td>
<td>1500ps</td>
</tr>
<tr>
<td>PDP(Power Delay Product)(Femto/sec)</td>
<td>1.764</td>
<td>2.364</td>
<td>2.537</td>
<td>6E-3</td>
<td>5E-4</td>
</tr>
<tr>
<td>EDP(Energy Delay Product) (Femto/sec)</td>
<td>5.21E-6</td>
<td>7.092E-9</td>
<td>7.611E-7</td>
<td>12E-11</td>
<td>10E-13</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>1.525mA</td>
<td>1.498mA</td>
<td>0.486mA</td>
<td>0.001mA</td>
<td>0.85 nA</td>
</tr>
<tr>
<td>PEP(Power Energy Product) (Femto/Sec)</td>
<td>6.098</td>
<td>1.812</td>
<td>2.137</td>
<td>5.4E-5</td>
<td>4.3e-5</td>
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</tbody>
</table>

Figure 7: Proposed Hybrid Full Adder Topology Carry
5. Conclusion

In digital design of submicron circuits, an internal logic circuit is proposed with the proposed approach to design and implement the circuit for efficient performances and analysis than the existing circuit. The proposed approach of the hybrid circuit provides faster process, less delay propagation, less power consumption and reduction in transistor count than the others. The DRPTL technology performance was with regard to the delay and power consumption of the submicron adder circuits used in digital circuitry. The MCSLA analysis was performed based on the area gate count. So the modified circuits satisfied VLSI requirements of an efficient submicron adder circuits.

References


