DESIGN OF 2.4 GHZ LOW POWER CMOS TRANSMITTER FRONT END

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Abstract: A high linearity low power low voltage direct conversion transmitter front end in 0.13µm CMOS technology is presented for 2.4GHz wireless sensor network (WSN) applications. It comprises an up conversion mixer, differential to single ended converter and power amplifier. Up conversion mixer is based on subharmonic passive mixer in which local oscillator takes the advantage of half of RF frequency. Differential to single ended converter is used to produce single ended signal from differential signals of up conversion mixer. To achieve 0 dBm transmit power, a current reuse power amplifier is designed at supply voltage of 1.2 V. The transmitter front end achieves 15dB conversion gain, output P-1dB of 0 dBm and -10.3 dB output return loss. It draws 4.27 mW power consumption.

Keywords: CMOS, subharmonic mixer, low power and Linearity

1. Introduction

Wireless Sensor Networks (WSNs) with the rapid development of semiconductor technologies have been growing in the field of medical and health care sectors [1,2]. Zigbee supports three ISM bands which are 868 MHz, 915MHz and 2.4GHz for low data rate, low power consumption and low cost applications in WSNs. Direct Conversion Transmitter (DCT) architecture is selected because it has many advantages of low cost, less area, easy integration and low power consumption [3,4]. The main drawback of DCT is Local Oscillator (LO) pulling problem where Power Amplifier (PA) output spectrum is equal to the LO frequency so that output spectrum of PA corrupts the LO signal [5]. For eliminating the LO pulling problem, LO frequency has to be far away from the PA output spectrum.

A single chip low power DCT comprises an up conversion mixer, differential to single ended converter and power amplifier stages. There are several CMOS based low power transmitter implementations that have been reported in the last few years. Nguyen et al implemented a low-power, high-linearity transmitter front-end by using a passive mixer and two-stage driver amplifier [6]. The driver amplifier consisted of conventional cascode amplifier as the first stage and the second stage used a folded cascode one to achieve 0 dBm output power. It consumed 5.4mW power under 1.8V supply voltage. Nam et al designed the direct conversion transmitter for achieving linearity, low offset and low carrier leakage by applying vertical NPN current mirrored technique [7]. It achieved >-2 dBm of output power at increased power consumption of 16.2 mW. A 915MHz low power CMOS RF transmitter which composed of up conversion mixer and driver amplifier was proposed [8]. The upconversion mixer was designed to eliminate the LO leakage at RF port. The cascode class A driver amplifier was designed to achieve the 0 dBm transmit power. The current consumption of the RF transmitter was 17.5 mA under a supply voltage of 1.8 V. A low-power, wide-range variable gain 900 MHz RF transmitter in 0.18 µm CMOS technology was presented [9]. It consisted of high linearity up conversion mixer and low power driver amplifier. This transmitter was consumed 4 mA current at a supply voltage of 1.25V. A low-voltage low-power transmitter front-end using current mode approach was presented [10]. Circuit techniques were employed for achieving low power power transmitter front end which utilized current mode circuits instead of voltage mode circuits to improve the linearity of transmitter front end at low supply voltage and low power of 5 mW. It achieved low power, but did not concentrate on drawbacks of transmitter. Due to CMOS scaling, the demand of low power, high linearity transmitter front end is increased. The transmitter front ends presented in the literature still dissipate high power while obtaining good performance and concentrating on the architecture’s drawbacks.

This paper describes the low voltage, low power CMOS transmitter front end for 2.4 GHz wireless sensor network applications. To achieve low power and high linearity transmitter, a passive subharmonic upconversion mixer which eliminates the LO pulling problem followed by differential to single ended converter and power amplifier are proposed. The paper is organized as follows. Section II describes the proposed transmitter architecture, system specifications of the IEEE 802.15.4 standard and the RF transmitter circuit designs. Section III summarizes the simulation
results of the transmitter and Section IV describes the conclusion.

2. Transmitter Specifications and Architecture

The RF transmitter specifications based on IEEE 802.15.4 standard are summarized in Table 1 [11]. IEEE 802.15.4 standard supports 2.4GHz with data rate of 250 kbps for DCT for WSN applications.

<table>
<thead>
<tr>
<th>Items</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulation</td>
<td>O-QPSK</td>
</tr>
<tr>
<td>Bit Rate [kbps]</td>
<td>250</td>
</tr>
<tr>
<td>Output Power [dBm]</td>
<td>&gt;-3 dBm or 0 dBm</td>
</tr>
<tr>
<td>OP1dB [dBm]</td>
<td>0</td>
</tr>
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</table>

A block diagram of direct conversion transmitter front end is shown in Fig.1. It consists of I/Q subharmonic passive mixer followed by single ended driver and power amplifier stages. This configuration is suitable to achieve low power and high linearity. The baseband or IF (intermediate frequency) inphase and quadrature (I/Q) signals are upconverted to RF I/Q signals by a subharmonic passive mixer. The RF inphase and quadrature components are added and are applied to differential to single ended converter which produces single ended RF signal. To achieve 0 dBm transmit power, the RF signal is amplified by driver and power amplifier stages with output matching network.

2.1 Subharmonic Up conversion Mixer

A schematic of passive subharmonic up conversion mixer is shown in Fig.2.
Subharmonic mixer takes the advantage of half of RF frequency to eliminate the problem of oscillator pulling and injection locking in direct conversion transmitter. It contains eight commutating switches which are formed as stacking of two switching quads where active devices work in deep triode region hence switches do not carry any DC currents and therefore do not cause flicker noise [12,13]. These switches are driven by quadrature LO signal i.e. LO signal is applied to the gate of the switching transistor. The baseband or IF differential signals are applied at the sources of LO switches. The commutating switches up convert the baseband or IF signal to the RF frequency signal.

The LO quadrature phases of sinusoidal signal is shown in Fig.3.

Let T be the full period of cycle. In the first quarter-cycle T1, the transistors M1, M1’ are on and M4, M4’ are on therefore the IF current flows to RF port. In the second quarter cycle T2, M1, M1’ and M2, M2’ are on therefore IF current flows to RF port but reversing the polarity. Each transistor is active for 50% of the full period of cycle T. Therefore, for a single cycle, the IF current is modulated four times and hence...
twice the LO frequency. Thus, subharmonic mixing of inphase component is obtained. Similarly, quadrature components of RF signal are obtained by quadrature LO signals which are π/4 phase shifted with respect to LO signals in the in-phase path. The drawback of passive mixer is its conversion loss. To minimize conversion loss, the width and biasing of switching quads are set properly.

The conversion gain of the passive mixer is calculated by time varying conductances of mixer switches. The output of the upconversion mixer is written as the product of three time varying components and a scaling factor as in Equation (1) [14].

\[
V_{RF}(t) = V_{RF}(t) \left[ \frac{\pi}{\omega_{LO}} \right] \left[ \frac{\pi}{2\pi} \right] \left[ \frac{g(t)}{g_{av}} \right]
\]

where \( g(t) \) is the time varying thevenin equivalent conductance at the RF port, \( g_{max} \) and \( g_{av} \) are the maximum and average values of \( g(t) \). The mixing function \( m(t) \) is defined as in Equation (2).

\[
m(t) = \begin{cases} \frac{\pi}{2\pi} \left[ \frac{\pi}{\omega_{LO}} \right] \left[ \frac{g(t)}{g_{av}} \right] & \text{for } m(t) > 0 \\ 0 & \text{for } m(t) = 0 \\ \frac{\pi}{2\pi} \left[ \frac{\pi}{\omega_{LO}} \right] \left[ \frac{g(t)}{g_{av}} \right] & \text{for } m(t) < 0 \end{cases}
\]

where \( T_{LO} \) is the period of LO drive. For sinusoidal LO frequency signal, the first bracketed term in Equation (1) has the value of \( \frac{\pi}{2} \) and the second bracketed term has the value of \( \pi/2 \). With a sinusoidal LO signal, the conversion gain (CG) of passive mixer becomes \( \pi/4 \) which is given by Equation (3) (Lee 1998).

\[
CG = \frac{\pi}{2}
\]

When compared with square wave LO drive, the conversion gain of passive mixer with sinusoidal LO drive has greater value. If the conversion gain has negative value, it is also called conversion loss. For subharmonic mixer, the conversion gain is defined as in Equation (4).

\[
CG = \frac{\pi}{2}
\]

2.2 Differential to Single Ended Converter

The subharmonic passive mixer produces inphase and quadrature components of RF signal which are added to obtain the differential RF signals. To produce single-ended RF signal, active balun circuit is designed as shown in Fig.4.

![Figure 4. Schematic of differential to single-ended converter](image)

It is used to combine the differential signals so as to form the single ended RF signal. It is composed of a two common-source (CS) (differential pair) stages M5 and M6 with load resistor R1 and R2 for RF+ and RF- signals respectively. Resistor \( R_s \) is used for tail current. The differential pair is designed so it would perform as a balun with unity gain. Therefore, the single ended output signal from the differential pair has the same amplitude as the balanced signal at the output of the mixer.

2.3 Power Amplifier

To achieve high gain, saturated output power and high linearity for ultra-low power and ultra low-voltage operations, output stages of transmitter are proposed as
shown in Fig. 5. Single-stage current reuse class AB power amplifier is designed. Current reuse structure has only one current path which supports low power consumption. In PA, the power stage is stacked at the top of driver amplifier. To support low power consumption, push pull amplifier and common source amplifiers are used as the driver and power amplifiers.

In PA, the driver and power stages are connected in current reuse structure to act as single stage power amplifier. It is operated under the supply voltage of 1.2 V. This supply voltage is sufficient for achieving 1mW output power of WPAN applications. The single ended RF signal is applied to driver amplifier. The driver amplifier has push pull inverter configuration which uses two common source transistors (M1 and M2) operating in parallel. To achieve higher power efficiencies without greatly sacrificing distortion performance, the class AB topology is highly desirable. Therefore, push pull driver amplifier is operated in class AB mode. Biasing is provided to maintain a low quiescent current through M1 and M2 (for class AB) operation when no input signal is present. The current flows in each transistor (M1 and M2) for less than the entire period of a sinusoidal input. The conduction angle of Class AB amplifier is between 180° and 360°. Class AB amplifier provides good efficiency and linearity. In addition, push pull configuration increases the total transconductances, therefore increases the voltage gain.

The total transconductance of push pull amplifier is given as [15],

$$g_m = g_{mn} + g_{mp}$$  \hspace{1cm} (5)

where $g_{mn}$ and $g_{mp}$ are the transconductances of NMOS (M1) and PMOS (M2) transistors. For this amplifier, the drain current is sinusoidal for one half cycle and a small portion of the other half cycle. The input matching network is achieved by inductor $L_1$, capacitors $C_1$ and $C_2$. To provide high impedance path for blocking the AC signal, the inductor $L_2$ is connected at the top of source of PMOS (M2) transistor. The driver amplifier output taken at the drains of M1 and M2 is given to the input of output stage through coupling capacitor $C_3$.

Output stage is a class AB common source power amplifier. Class AB amplifier is more power efficient than class A amplifier and is suitable for low power applications. Class AB amplifier provides better linearity across full input and output range than class B amplifier. The transistor (M3) of output stage is operated as a dependent current source. The suitable bias voltage ($V_{b3}$) has been chosen in class AB range. The capacitor $C_4$ is used for producing reliable AC ground. Inductor $L_3$ is used to provide the DC feed for the output stage. The output matching network consists of $C_5$ and the parallel network formed by $L_p$ and $C_p$ to match to 50 Ω load. The parallel-resonant circuit is also used as a band pass filter to suppress harmonics and select a narrowband spectrum of a signal. It is
resonated at the frequency of $\omega_0 = \sqrt{L_p C_p}$. The coupling capacitor $C_5$ is high enough so that its ac component is nearly zero. For common source amplifier, the small signal voltage gain depends on its transconductance and load impedance. The current reuse power amplifier has only one current path from VDD to ground. This structure reduces the current consumption.

3. Results and Discussion

The transmitter front end is designed in TSMC 0.13 µm CMOS process. The circuit schematic of transmitter front end is shown in Fig.5.

The layout of transmitter front end is drawn using Cadence Virtuoso as shown in Fig.6. It has an active area of 1257 µm $\times$ 712 µm.
The 5 MHz IF signal and 1.2 GHz LO signal with input signal level of -15 dBm and -5 dBm are applied as the input signals for upconversion mixer. Fig. 7 shows the overall conversion gain of the transmitter front end versus IF power. The pre- and post-layout simulation produces the conversion gain of 15.5 dB and 15 dB when the LO power is -5 dBm and consumes 4.27 mW power consumption under the 1.2 V supply voltage.

For transmitter, output return loss (S(2,2)) of -11 dB and -10.3 dB are obtained for pre- and post-layout simulation as shown in Fig. 8. The output return loss indicates the good RF output matching condition.

Also, transmitter front end has achieved the -0.915 dBm and 0 dBm of OP1dB for pre- and post-layout simulations as shown in Fig. 9.
Table 2 compares the performances of transmitter with the existing work.

**Table 2. Performance comparison of transmitter front ends**

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Wann and Wang (2011)</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (MHz)</td>
<td>900</td>
<td>2400</td>
</tr>
<tr>
<td>LO Power (dBm)</td>
<td>0</td>
<td>-5</td>
</tr>
<tr>
<td>Output Power (dBm)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Conversion Gain (dB)</td>
<td>16</td>
<td>15</td>
</tr>
<tr>
<td>OP-1 dB (dBm)</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>5</td>
<td>Passive Mixer : -</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single to</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Differential</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Converter : 0.93</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PA : 3.34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total : 4.27</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
<td>0.8-1.2</td>
</tr>
<tr>
<td>FOM (dB/mW)</td>
<td>3.2</td>
<td>3.51</td>
</tr>
</tbody>
</table>

In [10], the transmitter post layout results are ±1 dB deviation of the measurement results which are presented in the Table 2. The power consumption has reduced at low LO power in the proposed transmitter. FOM is calculated by the ratio of gain to the power consumption. The performance of proposed work is compared with the existing work by FOM. Though, the FOM of proposed transmitter is very slightly increased than existing work, the proposed transmitter has mitigated the LO pulling problem. The transmitter has achieved 0 dBm output power at 4.27 mW dc power consumption.

4. Conclusion

A low power 2.4 GHz RF direct conversion transmitter front-end for WSNs has been designed in TSMC 0.13 µm CMOS technology. With the main goal of low power and high linearity, a subharmonic passive mixer showed very good performance to convert the baseband signal directly to a RF signal. A single ended driver and push pull power amplifiers are used to obtain 0 dBm transmit power. The transmitter attained 15 dB conversion gain and 0 dBm output P-1dB. With the proposed circuit design techniques, the RF transmitter front end consumed 4.27 mW power.
References


