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Coordinate Rotation Digital Computer Enabled Built-in-Self-Test Scheme for Oversampling Analog-to-Digital Converter

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Abstract

Objective of this paper is to design and extract the offset error, Gain error, DNL, INL,SNR parameters of oversampling Analog-To-Digital Converter (A/D) by using CORDIC technique. Mathematical concept of COordinate Rotation DIgital Computer (CORDIC) is used as reference histogram for evaluation of performance parameter in sigma delta based ADC. The circuit under test (CUT) is a sigma delta modulator planned by utilizing SIMSIDES. SIMSIDES (SIMULINK-based Sigma-Delta Simulator) is a MATLAB SIMULINK device having S-work squares utilizing Switch capacitor(SC) procedure. Discoveries are exceptional and novel in light of the fact that CORDIC is first time acquainted with get ADC static and dynamic parameter. Here high light of our result is that using CORDIC high SNR_d is achieve and Circuit complexity is removed. It is helpful contribution in the field of mixed signal IC's testing and significantly reduce the design cycle time of IC fabrications. Oversampling ADC are widely used in application of Audio application ,Industrial Application ,Modern wireless communication, CMOS image sensor due to high resolution and great accuracy compare to nyquest ADC.

Index Terms: CORDIC, ORA, SDM ADC, CUT,BIST,PEC.

1. Introduction

Analog-to-digital Converter (ADC) is generally utilized as a mixed signal device in many of the system-on-chip designs. Presently a day[1,2], a pattern toward incorporating the system-on-chip framework onto a solitary chip is in demands . So with diminished size, cost and power utilization, the advancement towards the improvement of new age of hardware foundational fulfilling every single significant component for the collaboration of constant world to the computerized handling hardware is in its extraordinary request [3,4].

The testing a VLSI chip to ensure its usefulness is especially unpredictable and regularly extremely time taking. Notwithstanding the trouble of testing the chips (IC) themselves, the consolidation of the chips into frameworks has caused test age's cost to develop highly [5, 6, 7]. The system to manage the testing issue at the chip level is to consolidate worked in individual test (BIST) ability inside a chip. This builds the controllability and the perceptibility of the chip [8,9,10] In regular testing, test designs are delivered remotely through the assistance of PC helped outline tools(CAD). The test designs and the normal reactions of the Design under test to these test designs are utilized via programmed test gear (ATE) to decide whether the genuine reactions same as the normal ones[11]. Then again, in worked in individual test, the test design age and the yield reaction estimation are done on chip; in this manner, the utilization of top of the line programmed test gear (ATE) machines to test chips can be avoided[12,13] High-determination ADCs with high examining rates are required in an expansive territory of superior applications, such as high-grade imaging systems, wireless correspondences, and radar [14,15]. The utilization of BIST procedures assuages the reliance on exorbitant test hardware and permits conveying minimal effort gadgets [16]. The coming of reconfigurable rationale of PCs allows the higher speed of committed equipment arrangements at the costs that are aggressive with conventional programming approach. Considerably more, the equipment proficient calculation is a class of iterative answer for trigonometric and other supernatural capacities utilizing just moves and adds to perform. The trigonometric capacities are primarily in light of vector revolutions; however different capacities are actualized by the utilization of incremental articulation in view of the coveted capacity[3,17]. The trigonometric calculation is called CORDIC (Coordinate Rotation Digital Computer).

Here, the focus is on the application of CORDIC (Coordinate Rotation Digital Computer) carried out by a MATLAB.The paper is organized as follows: Section 2 is a related works. Section 3 deals with proposed work. Section 4 result and discussion. Section 5 tells about the conclusion and future work.

2. Related Works

Sigma-Delta Converters

Sigma delta Modulator based converters work at oversampling Frequency. That implies the testing recurrence is substantially more noteworthy than message frequency (Fm). Contrasted and Nyquist rate ADCs, oversampling ADCs gets high determination notwithstanding simple segments it utilizes advanced flag preparing for changing over simple to-computerized conversion[18,19] and because of the oversampling sigma-delta ADCs; they don't required roll off filter , [20]which is the prime prerequisite of nyquist rate ADCs. In this way, higher request with better and higher linearity are no utilized and by and large evaded to clear up why the examination was attempted and what speculations were tested[21]. In earlier research the hardware design of Analog to digital world standardized commonly by languages such as VHDL and Verilog. Lately, there has been a growing interest in alternative languages for coding at a much higher level of abstraction. System C, and System-Verilog represent the most widespread language Figure 1. shown below . These languages equipped with well-known syntax with powerful constructs, enabling the realization and simulation of huge complex systems; in specially System C has grown up and become popular[22].

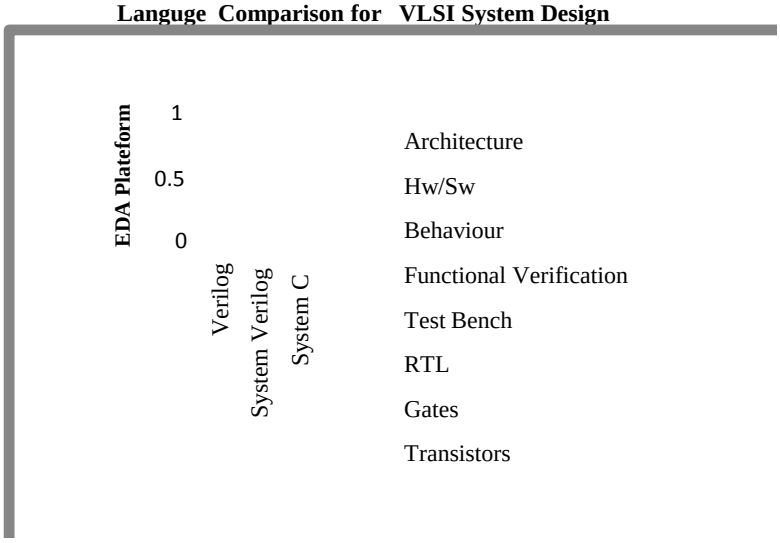

Figure 1. Language Vs Hardware EDA Platform Realization

Polynomial Approximation

An alternative approach for the approximation of arbitrary function for closed intervals by using polynomial can also be used. However, in this approach pre determination of derivatives are required but is frequently unavailable. Moreover, when the given data are large the calculation for the matrix is very complex as well as a long operating time will be necessary.

CORDIC Technique

The advent of reconfigurable logic of computers permits the higher speed of dedicated hardware solutions at the costs that are competitive with traditional software approach. Even more, the hardware-efficient algorithm is a class of iterative solution for trigonometric and other transcendental functions using only shifts and adds to perform. The trigonometric functions are mainly based on vector rotations, but other functions are implemented by the use of

incremental expression based on the desired function. The trigonometric algorithm is called CORDIC (Coordinate Rotation Digital Computer).Table 1 shows Comparison of different methods available for testing technique.

Table 1. Comparison Tables of the Above Methods

Technique	Cost	Complexity
Maclaurin Series	High	More
Polynomial Approximation	Moderate	More
CORDIC technique	Moderate	Moderate

PROBLEM IDENTIFICATION

This section identifies and formalizes the problem faced while implementing the references.

Problem Statement:

- After surveyed the paper it is compressed that there are a few confinements in the process taken. Some of them are:
- BIST strategy has not been executed for the sigma delta acquired from SIMSIDES.
- The estimation of static parameters and SNR is less in the majority of the cases, which isn't wanted.
- Computational time is more.
- The extensive memory limit is required in the circuit.
- Model recreation isn't right due to the non-Linearity.
- On chip overhead range is more.

Objective

- To design and extract the following parameters of sigma delta modulator:Offset error, Gain error, DNL ,INL,SNR.
- To test the improved output of a switched capacitor second order sigma delta modulator, designed in SIMSIDES by using CORDIC technique.

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3. Proposed Work

Circuit Under Test (CUT)

The circuit under test (CUT) is a second order sigma delta modulator designed by using SIMSIDES. SIMSIDES (SIMULINK-based Sigma-Delta Simulator) is a MATLAB SIMULINK tool having S-function blocks using switched capacitor technique.

Output Response Analyzer (ORA)

The ORA of the BIST framework has been planned by utilizing Coordinate Rotation Digital Computer (CORDIC) system. This system is connected to build up the sine wave reference histogram on chip with adequate precision.

The Basic CORDIC Technique

Figure 2 indicates graph of fundamental CORDIC Technique in which gives an iterative plan to assess numerous basic capacities, similar to logarithm, Trigonometric capacity and division, utilizing a move and-include strategy.

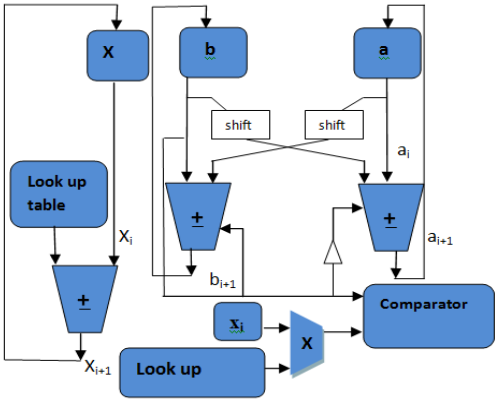

Figure 2. Block View of basic CORDIC Technique

Code/Counting Assignment

Table 2 shows Algorithm for Sample_cnt and Table 3 shows Algorithm: Counter [code counting].detail of description are as below:

- Code_cnt: The modulator's output code is

captured, analysed and indicated by this counter, viz 0 to 2N-1.

- Sample_cnt: Represents the total number of samples for each code. For each code, it counts from 0 to Nt-1.

Table 2. MATLAB Algorithm For Sample_cnt

```
dt = 1/Fs;                                          %seconds per sample
        StopTime = 1;                               % seconds
N = size(t,1);                                      %  Sine wave:
          Fc = 12;                                  % hertz
x = cos(2*pi*Fc*t);                                 %Cos Function
          Fourier Transform: X = fftshift(fft(x));  % Frequency
specifications:
dF = Fs/N;                                          % hertz
          f = -Fs/2:dF:Fs/2-dF;                     % hertz
Plot the spectrum:
figure;
           plot(f,abs(X)/N);
           xlabel('Frequency (in hertz)');
           Title('Magnitude Response');
```

Practical Code Counting (PCC)

- **Code_sta**: Connected to the modulator's output directly. The practical sine wave histogram of the code is computed using counter. As long as the modulator's output is identical to the present value of the Code_cnt, the counting for number of blocks will be increased. If the value of Code_cnt is changed, this increment will stop.

Table 3. Algorithm: Counter [code counting]

```
N=1000;
            c=[2 3 5 7];
counter=1;
             for x=1:N
V=mod(x,c);
F=V(V==0);
            if isempty(F)
Prime(counter)=x;
counter=counter+1;
else
continue;
end
end
```

CORDIC-based Reference Histogram Calculator

Table 4 shows CORDIC Algorithm used as reference histogram for evaluation of performance parameter in sigma delta based ADC.The steps are as follow:

- **Input_set:** A Multiplexer (MUX) which chooses the usefulness of the CORDIC piece to perform.
- **CORDIC:** An inserted CORDIC histogram calculator. Capacities, for example, the converse sine capacity and division can be computed.
- **Reg:** Two registers to store the intermediate computing values for saving the area overhead. Further, the cost will be diminished when contrasted with the strategy utilizing an additional memory.
- **Offset_cal:** The input offset error can be evaluated. Input_cal: Various input parameters are calculated using this block, when the output of Code_cnt is increased.

- **H_ref:** This piece is utilized to assess the last estimation of the sine wave histogram for the code.

Table 4. Algorithm for CORDIC

```
function [x, y, z] = cordic_rotation_kernel(x, y, z, inpLUT, n)
   % Perform CORDIC rotation kernel algorithm for N iterations.
xtmp = x;
ytmp = y;
            for idx = 1:n
           if z < 0
                        z(:) = accumpos(z, inpLUT(idx));
       x(:) = accumpos(x, ytmp);
       y(:) = accumneg(y, xtmp);
else
         z(:) = accumneg(z, inpLUT(idx));
         x(:) = accumneg(x, ytmp);
          y(:) = accumpos(y, xtmp);
end
xtmp = bitsra(x, idx); % bit-shift-right for multiply by 2^(-idx)
ytmp = bitsra(y, idx); % bit-shift-right for multiply by 2^(-idx)
end
```

Table 5. Comparison Table

S.N.	**Parameter**	**Ref.[3]**	**Ref.[9]**	**Ref.[12]**	**This Work**
1.	**[Accuracy]**	Low	Medium	Medium	High
2.	**Simulation Speed**	Average	Good	High	Very High
3.	**Complexity**	Very High	Medium	Medium	Less
4.	**SNR**	0.860	0.87	0.92	0.95
5.	**Data-bit width**	13 bit	13 bit	13 bit	13 bit

Parameter Evaluating Circuit(PEC)

- Parameter_out: This block is used to calculate the static parameters of the Sigma-Delta modulator using the output of the Code_cnt, H_ref as well as CORDIC block shown in figure 3. The static parameters which can be calculated are offset error, gain error, DNL, INL and Dynamic parameters like SNR.

With the above description the proposed block diagram for the design of ORA for BIST of Sigma Delta Modulator can be given in Figure 3.

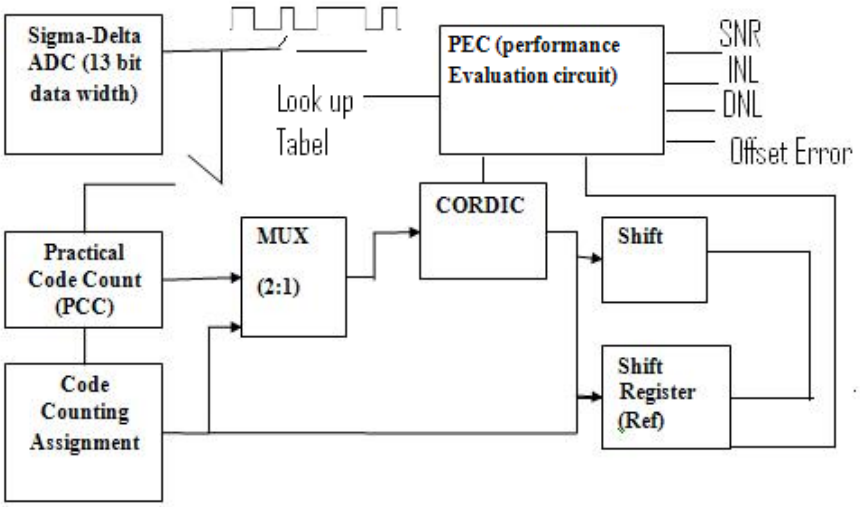

Figure 3. Proposed CORDIC enable ORA for BIST

4. Result and Discussion

This section exhibited the trial setup and the consequences of the reenacted demonstrate .This segment starts with a talk of the parts required in the test setup. The segment at that point displays the outcome got. At long last, finishes up by an exchange and examination of the outcome acquired by considering required execution markers like DNL, INL and SNR appeared in figure 4.

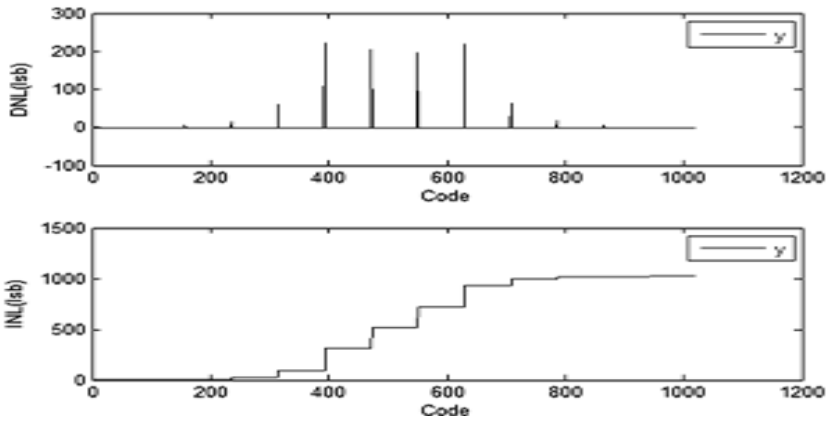

Figure 4. SIMSIDES Computation of INL and DNL

BIST Output:

The SIMSIDES output is given to the ORA of the BIST Circuit and the testing parameters are obtained in Figure 5 and is comparative analysis is reported in table 4 as well as figure 6.

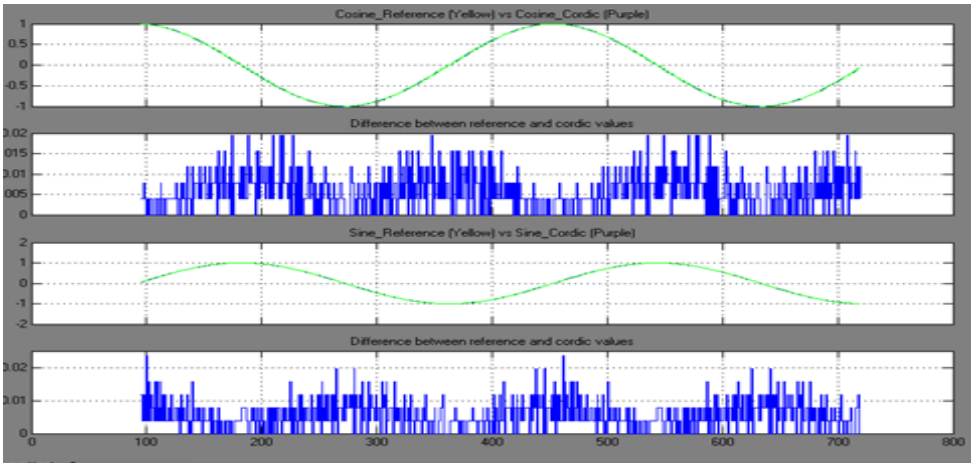

Figure 5. SIMSIDES ORA Response of calculated for Test Pass or Fail

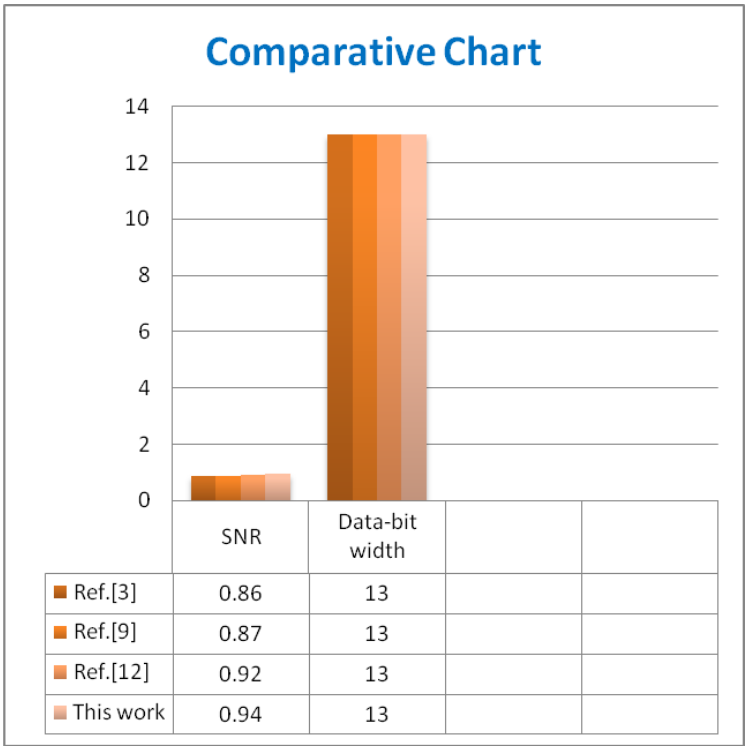

Figure 6. Shows Comparative result

5. Conclusion and Future Work

This can be seen with the assistance of results section and the talks that the work is region productive and better execution is come about with enhanced the Resolution and Signal to Noise Ratio (SNR). Acknowledgment of framework level Hardware model of BIST with second order low-pass sigma-delta modulator plan under test has been accomplished. The modulator's static and dynamic parameters i.e. Quantization error, pick up mistake, DNL, INL and SNR are gotten utilizing sine wave histogram test and are figured utilizing the proposed ORA circuit based on CORDIC approach. The parameter mistakes and equipment cost for the acknowledgment intention are being ascertained. Subsequently, the precision of the proposed innovation is extensively high. Since the proposed innovation is completely a computerized circuit Because of Mathematical concept of COordinate Rotation DIgital Computer (CORDIC) is used as reference histogram for evaluation of performance parameter in sigma delta based ADC. subsequently, the execution of the modulator ORA won't be corrupted.

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