

PERFORMANCE ANALYSIS OF ADDERS USING TRANSMISSION GATE LOGIC

Sakthi Kumar B¹, Venkata Surya Vamsi Manda², Sai Ranadheer Gupta Nunna³,
Amrutha Lakshmi Devi Sandu⁴, Dinesh Uppala⁵

¹Department of Electronics and Communication Engineering,
Koneru Lakshmaiah University, Guntur, India
suryavamsi.m@gmail.com

Abstract: In the paper, various adder circuits are implemented using 16-Transistor CMOS Transmission Gates full adder cells. The simulated results of different adders designed using the above full adder cells are compared with each other. The quantity of transistors are diminished from 28 to 16 for designing full adder cell.

Keywords: Adder, Transmission gate, Full adder, Tanner.

1. Introduction

The basic integrates to today's high-end application processors are adders. A Full Adder is the basic entity of these circuits [1]. Hence, elevating its conduct elevates the whole circuit's conduct.

A full adder is to be viewed as a 3:2 lossy compressor as it gets 3 binary bits as input (including the carry input) and produces 2 binary bits as the output (including the carry output).

Transmission gates can be expounded as electronic elements that discerningly either pass or block the signal through input to output. Transmission gate comprises of PMOS transistor and NMOS transistor [2]. It is designed by connecting both drain to drain and source to source terminals of NMOS and PMOS transistors respectively. n-channel of this gate is responsible for the correct transmission of the logic zeros and the p-channel of this gate is responsible for the correct transmission of logic ones [3].

A full adder adds 2 binary bits with a carry input and fabricates 2 results specifically, Sum and Carry output.

Table 1. Truth Table for a Full Adder

Inputs			Outputs	
A	B	C _{in}	Sum	C _{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The expressions to calculate the Sum and Carry out values of a full adder are given as

$$\text{Sum} = A \text{ xor } B \text{ xor } C_{in}$$

$$\text{Carry} = (A \text{ and } B) \text{ or } (B \text{ and } C_{in}) \text{ or } (C_{in} \text{ and } A)$$

There are different styles and logics to implement different Adders based on the requirement of power, area and other aspects [4]. Each logic makes beneficiary on different aspects though any logic may not be able to fulfil all the aspects as required. Hence, each design is one of its kind.

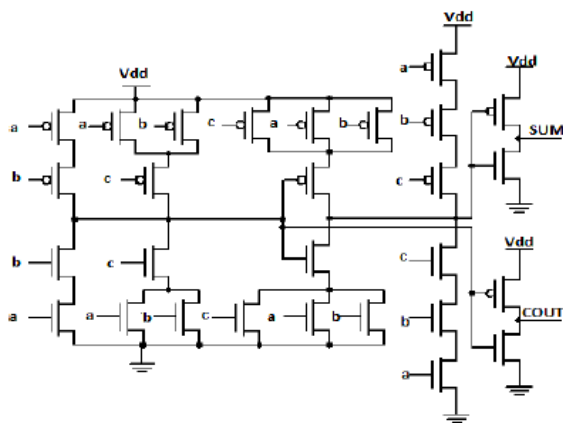


Figure1. Standard Full Adder Circuit

The standard full adder circuit shown in Figure.1 is a complementary CMOS full adder with 28 transistors consisting of both PMOS pull up transistors and NMOS pull down transistors [5]. It is greatly found with scalability at low supply voltages.

2. Ripple Carry Adder

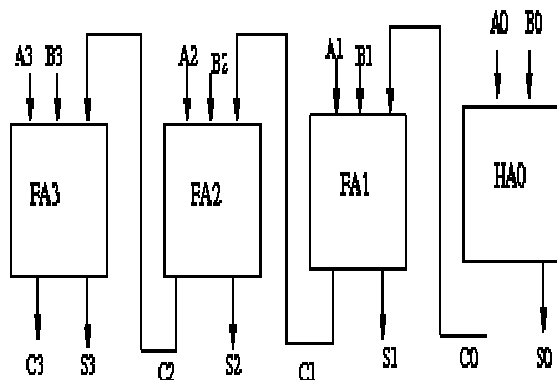


Figure 2. Schema for Ripple Carry Adder

It is possible for adding N bit numbers by cascading N full adders parallelley [6]. In Ripple Carry Adder, the output carry of individual full adder is carry in for its succeeding adder i.e., each carry bit “ripples” to next adder [7]. In this circuit, the carry out bit and sum bit at half adder stage is not authentic until input carry for that stage occurs. Propagation delays inside the logic circuitry is the reason behind this.

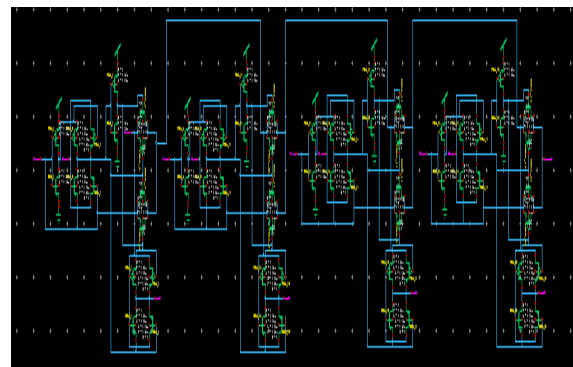


Figure 3. Schematic of Ripple Carry Adder

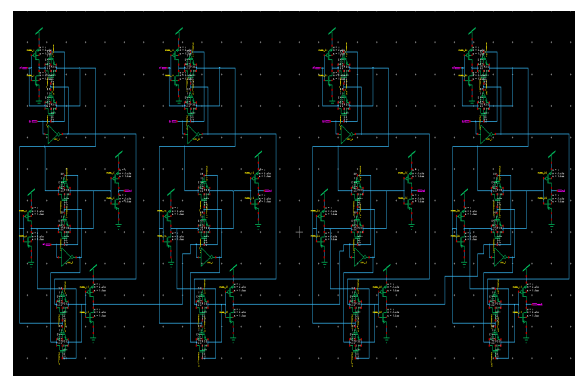


Figure 4. Transmission gate Ripple carry adder

3. Carry-bypass Adder

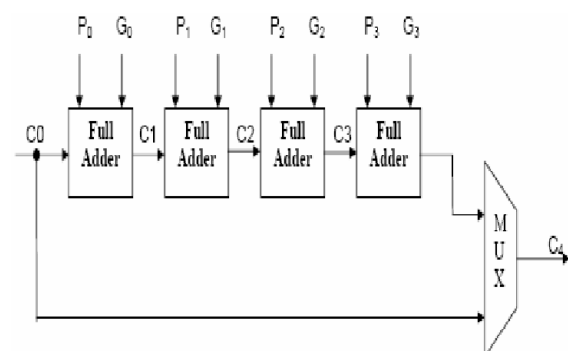


Figure 5. Block Diagram of Carry-Bypass Adder

Carry-bypass adder, also referred as Carry-Skip Adder is an adder implementation that improves delay for a ripple carry adder [8].

The propagate generated from each adder is given by equation

$$P_i = a_i \text{ xor } b_i$$

where a,b are the input bits of the respective adder. These propagates are used to generate the select bit of the Multiplexer.

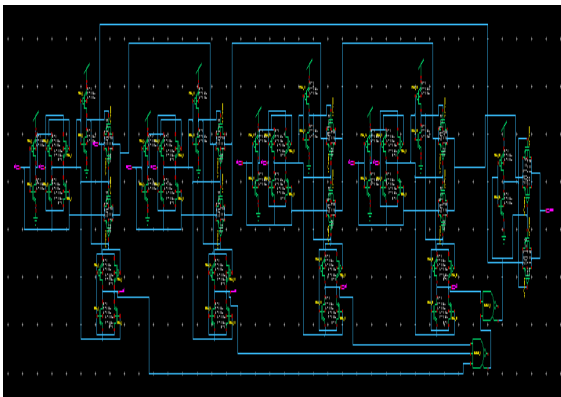


Figure 6. Schematic of Carry-Bypass Adder

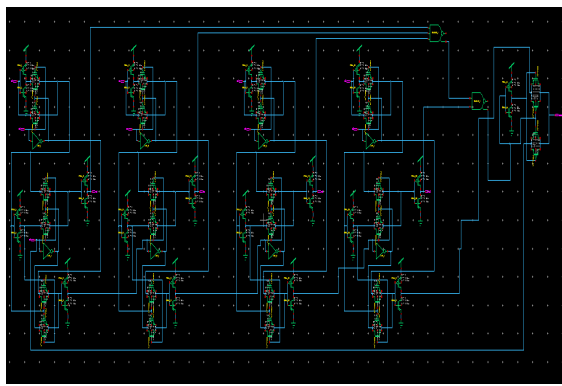


Figure 7. Transmission gate Carry-Bypass adder

4. Carry-save Adder

The Carry-save adder is sort of adder applicable for the microarchitecture in computer for computation of sum of n -bit numbers. Carry Save Adders can be used in Booth's Multipliers [9]. For an $n \times n$ bit multiplication, it requires n partial products and each partial product requires $n/3$ n -bit carry save adders. Both the full and half adders have used for a Carry Save Adder.

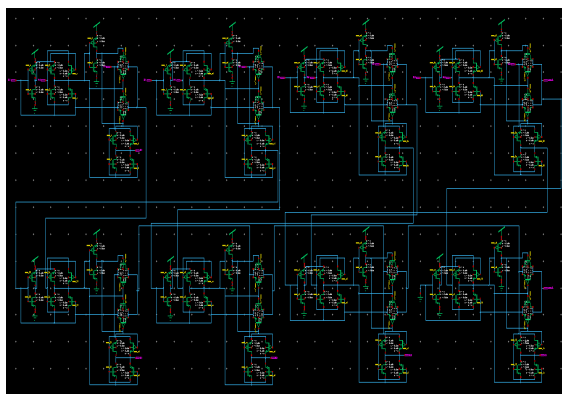


Figure 8. Schematic of Carry Save Adder

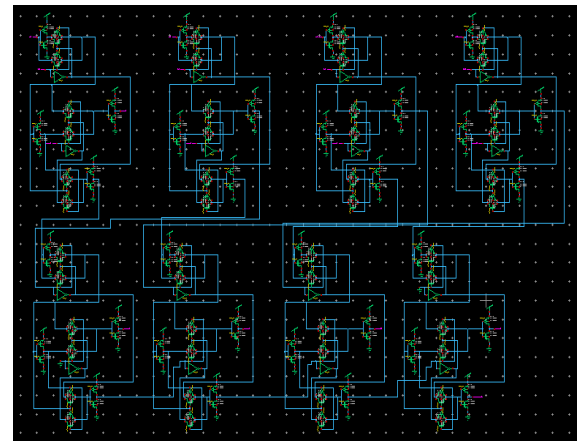


Figure 9. Transmission gate Carry Save adder

5. Schematic Analysis

Schematic of proposed full adders has following device and node counts:

Table 2. No. of MOSFETs used

Adder	MOSFETs		
	Conventional	Transmission Gate Logic	Hybrid Logic
Ripple Carry Adder	112	96	64
Carry-Bypass Adder	148	116	84
Carry Save Adder	224	192	128

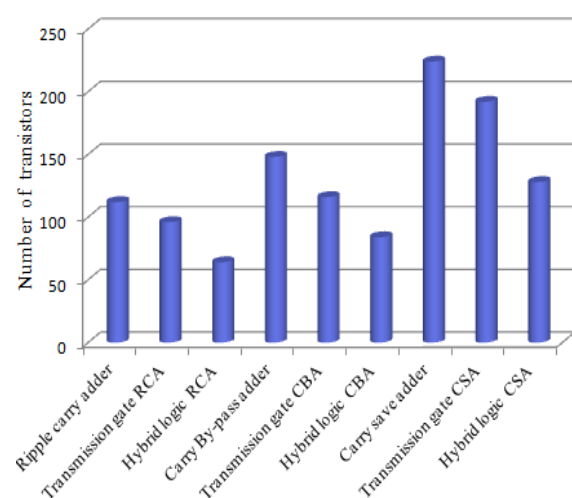
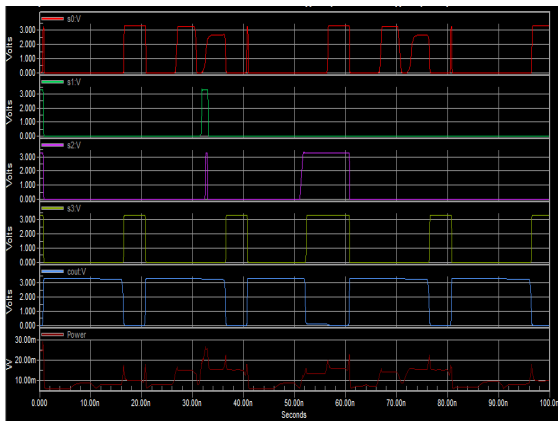
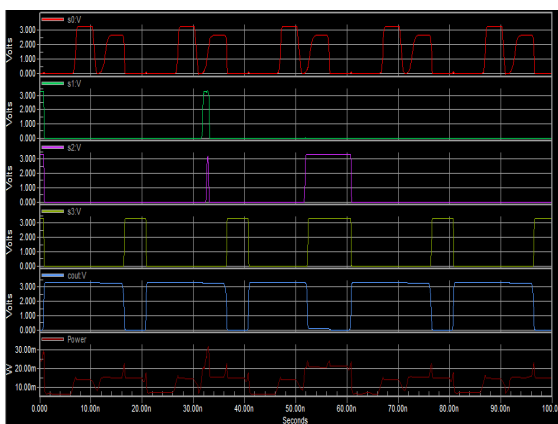
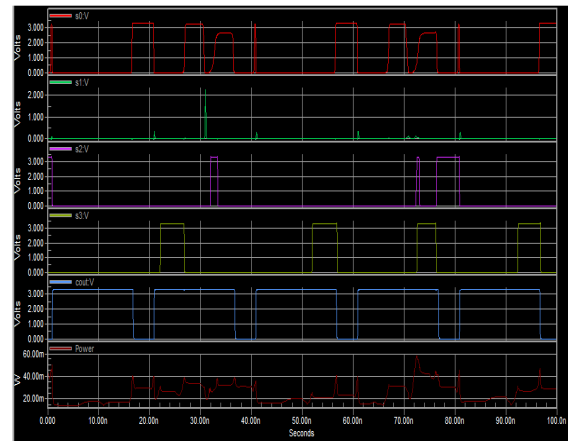


Figure 10. Transistor Count of Adders**6. Results****Table 3.** Average Power Consumed

Adder	Average Power Consumed		
	Conventional	Transmission Gate Logic	Hybrid Logic
Ripple Carry Adder	10.467 mW	21.2 mW	9.486 mW
Carry-Bypass Adder	13.281 mW	22.03 mW	10.44 mW
Carry Save Adder	24.527 mW	28.97 mW	17.05 mW

**Figure 11.** Simulation of Ripple Carry Adder**Figure 12.** Simulation of Carry-Bypass Adder**Figure 13.** Simulation of Carry Save Adder**7. Conclusion**

The transistors expected to design a complete adder have been reduced from 28 Transistors to 16 Transistors using the Transmission Gate Logic and various kinds of adders have been designed and simulated based on these full adder cells. These various kinds of adder circuits have been implemented using 16-Transistor CMOS Transmission Gates full adder cells. The simulated results of these different adders designed using the above full adder cells are compared with each other. After comparing among Conventional, Transmission Gate based and Hybrid (combination of the above two) logic, it may be concluded that those Adders designed using the Hybrid logic are having the less Transistor count as well as they are consuming less Power when compared to the other two types.

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