

DESIGN FOR VEDIC MULTIPLIER USING TRIPLE FAULT TOLERANT ADDER ARCHITECTURE

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Abstract - In this paper, we present the multiplier circuit using fault tolerant adder circuits, in this system the fault and increase the reliability of the multiplier circuits will be reduced. Simultaneously fault will be occurring and area overhead and many faults will be tolerant in the multiplier circuit in the design implementation. In this paper the vedic multiplier circuits using fault tolerant adders are presented. The synthesis the methodology of multiplier coded in Verilog HDL. ISim 11 is used to perform the resultant simulations. The usage of area and power consumption were obtained by suing the software Xilinx ISE 11.

Keywords: Test Pattern, Fault tolerant, Vedic multiplier, Low power.

1. Introduction

The main difficult areas in VLSI are overall performance, fee, testing, area, reliability and power dissipation. Switching activity increases the power dissipation i.e. the power ate up trying out, due to quick current in the circuit waft and being able to charge the load area, strength and reliability. The demand for transportable computing devices and communications gadget are growing swiftly. The packages require low strength dissipation VLSI circuits. The energy dissipation throughout check mode is two hundred% greater than in everyday mode . As a result, the critical issue to optimize power all through testing The capacity to layout, fabricate and test application precise incorporated Circuits (ASICs) as well as FPGAs with gate

remember of the order of some tens of tens of millions has caused the improvement of complicated embedded SOC. The external implication of hard ware additives requires more processors in SOC. Reminiscences and committed additives for expedite crucial responsibilities and alloy to numerous item. One of the best method for soc design is primarily method. As an instance, the platform FPGAs which includes Xilinx Spartan three Excalibur consist of customized for a good analysis of dives, fixed programmable processer contain millions of gates. 4 motives are blamed for energy growth for the duration of check:

- High-switching hobby because of type of test styles,
- Simultaneous stimulation of inner cores in the course of check,
- More power full DF5T circuits are using
- Test vector correlation will be very low

The energy dissipation of machine is very high in look at mode comparing to normal mode [13]. Less successive checks require less amount for patterns applied for scan chains. Improve divert pass time in scan chain then out comes power also increasing in experiment and combinatorial block [4]. This additional power consumption may create complication together with spontaneous power rise; because of this block will be harm. Some black sports are formed due to this additional power, this causes the complication in execution, testing. And

also reducing the block output and life time. Different methods are present to improve power [13]. Those include innovation for test requires minimal power. This are using step down average and top power. Strategies for decreasing strength in the course of test checking out and TPG (integrated-self-test) technique. FPGA and bounded presences will be creeping than off-chip.so that it will limit the period compulsory for modifying of p of the criterion in TPG, take a look at method the use of layout for testability approach is proposed for this example.

2. Related Work

Different methods are find the fault and different multiplier circuits reducing delay and power dissipations. The fault tolerant technique applied in adder circuits and then the adder applied in multiplier circuits. The vedic multiplier circuits for reducing area, delay and power dissipations of multiplier circuits. the below circuits mention the test pattern generators and adders.

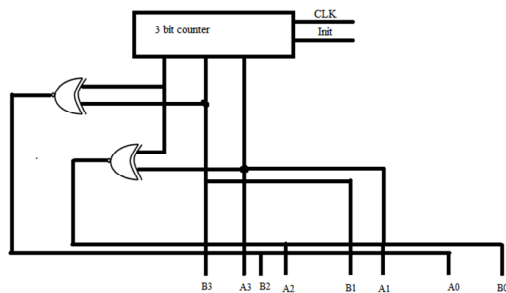


Figure 1. Test pattern Generator

The initial input reset the counter outputs. Here we are using 3 bit counter circuits. the counter output signal produce the test pattern adder input depends on clock signals. The initial condition zero means the counter circuits activate and they give the input vectors signals to the adder circuits.

Table 1:

	A	B	A	B	A	B	A	B	A	B	S	S	S	S	C	C
4	4	3	3	2	2	1	1	0	0	4	3	2	1	0	1	0
0	0	0	1	1	0	0	1	1	0	0	1	0	1	0	1	1
1	0	1	0	1	0	1	0	1	0	1	1	1	1	1	0	0
2	1	0	1	0	1	0	1	0	1	0	1	1	1	1	0	0
3	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0	0

4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	1
6	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	1
7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

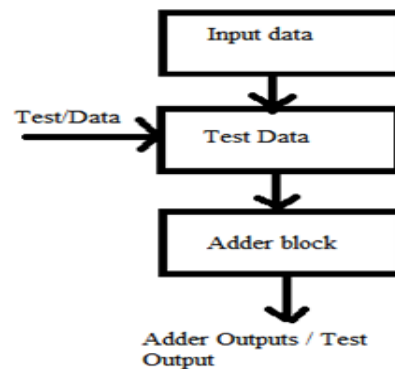


Figure 2. Test Adder

3. Fault Tolerant Adder

A simple RCA adder consists of full adders. The sum and carry signals are affected by faults. The carry signals internal to the RCA adder. For testing the full adder completely 8 test vectors are required and if there was a faulty full adder, then at least one of the two sum signals in the full adder and its succeeding cell will also be fault resultant. Because we are not checking the carry signals with the hardware checker. The detection of fault should be observable and controllable for each intermediate full adder cell and for the purpose of reconfiguration.

The one dispensable Full adder is used with four working Full adder and in testing phase the fault is detected. At the input and output levels the full adder function is bypassed by the spare one using multiplexer. the test pattern output signals are A_i, B_i, C_i . For i =odd and i =even The A_i signals are identical. It is also same for B_i, C_i and S_i . A 3-bit counter and some few combinational gates and are required for the generation of testable vectors as shown in figure 1.

In the MUX the carry and select lines are AND with the Data/Test line for which the same carry is given for all the full adders to carry its Inputs. The function of all the full adders are checked

by the test vectors which are fed to them and then compared with the desired on that was generated using the simple combinational circuit. The lookuptable of size 2×8 stores the desired outputs. The S0,S1 are compared with all the generated outputs which are stored by the lookup table. The test vectors requires 8 clock pulses and compare with the output vectors. the identification of faulty full adder depends upon the result given by the comparator and by the selection signal in the corresponding MUX will generate the proper input an output.

4. Vedic Multiplier

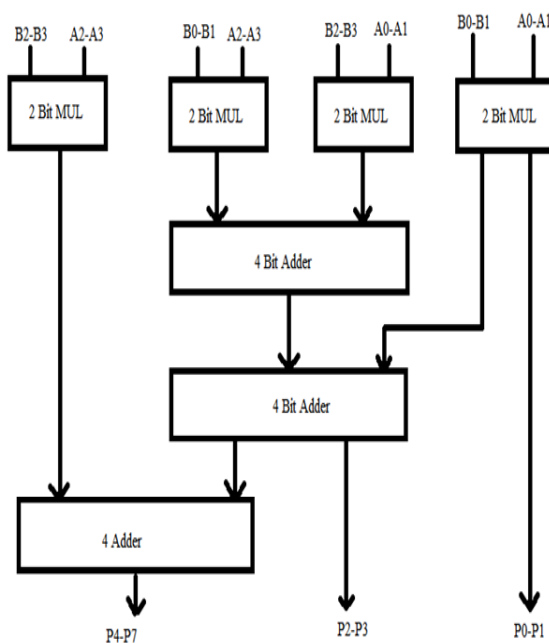


Figure 3. Vedic Multiplier

Multiplication is most important circuit for Arithmetic unit in Signal processing applications. Here we are proposed 4 bit Vedic multiplier using fault tolerant Adder circuit. So we find the fault tolerant of multipliers circuits. The 4×4 multiplication has been done in a single line in UrdhvaTiryagbhyam sutra [1], whereas in shift and

add (conventional) method, four partial products have to be added to get the result. Thus, by using UrdhvaTiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier. The two bit multiplier outputs are give to 4 bit Faulty tolerant adder circuits. the adder circuits generate the multiplier outputs signals.

5. Results

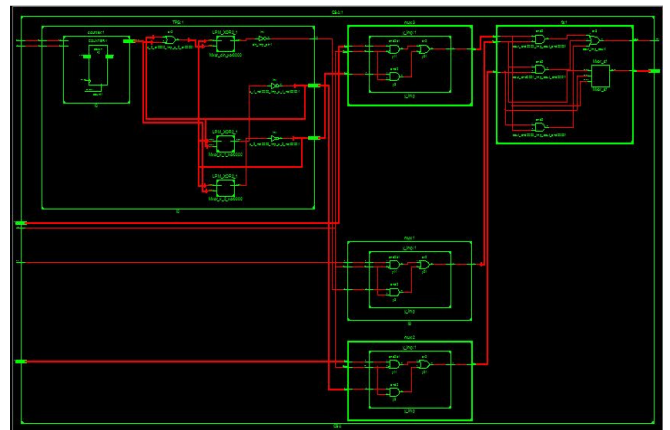




Figure 6. Adder waveform

Here in the above taken results the fault tolerant outputs and multiplier outputs are mentioned. The test signal when it is 0, the multiplier is time varies from 0 ns to 200 ns and they generate the multiplier outputs.

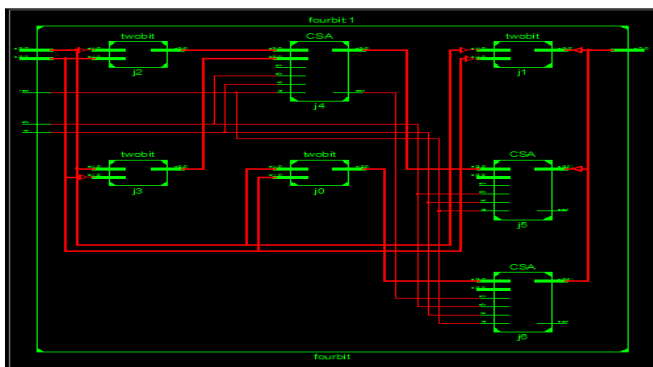


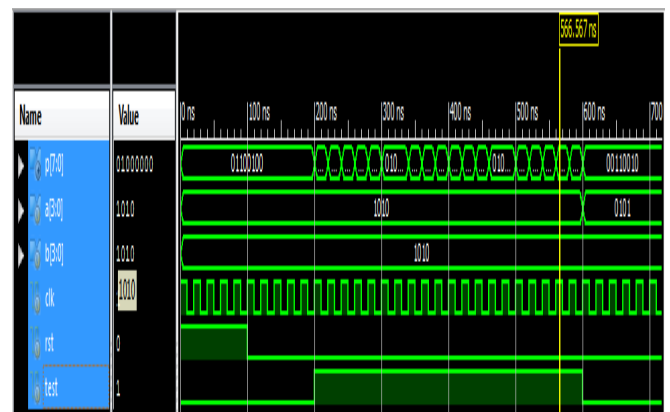
Figure 7. RTL Design for Adder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	34	704	4%
Number of Slice Flip Flops	9	1408	0%
Number of 4-input LUTs	60	1408	4%
Number of bonded IOBs	19	108	17%
Number of GCLKs	1	24	4%

Figure 9. Multiplier Waveform

Figure 8. Synthesis Report for Adder

After test input is 1, 200 ns to 600 ns the multiplier generate the test pattern multiplier outputs. The test signals will be generated from the eight periodic clock signals.



In this result mention the multiplier outputs and fault tolerant outputs. The test signals 0 The multiplier 0 ns to 200 ns they generate the multiplier outputs. After test input is 1, 200 ns to 600 ns the multiplier generate the test pattern multiplier outputs. The eight clock signals period the generate the test signals.

6. Conclusion

The proposed designs had the limit of distinguishing the flaws which occurs in the combinational circuit. The unmarried enter exchange styles produced enhance the connection among the progressive test subsequently diminishing force prerequisites. The proposed method find the fault tolerant in multiplier circuits. The power analyzer utilizing Xilinx 11 ISE programming.

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