

ESTIMATOR FOR CONTROL LOGIC IN HIGH LEVEL SYNTHESIS

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Abstract: The behavioral description is transformed into Control Data flow Graph (CDFG). The obtained CDFG is converted into Behavioral Network Graph(BNG). According to state cut the Behavioral Network Graph is used to estimate the hardware required for control construct alone is estimated. The state cut is decided by the number of hardware resources available. The AND gate and OR gate is estimated with matrix representation which is done for CDFG. An estimator is designed for control construct alone.

Keywords: Hardware estimator, High Level Synthesis, Logic Synthesis, Behavioral Network Graph.

1. Introduction

The hardware estimation in High level synthesis and register transfer level model is quite different because each model uses different intermediate representation. It leads to un optimized estimation, In order to obtain optimized estimation it requires same intermediate representation for both High level synthesis and register transfer level model. Normally RTL network is given to the logic synthesis for gate level optimization. The optimization depends on both the tools. To predict hardware in High level synthesis, it depends on scheduling, allocation and resource sharing in algorithmic level which will have on final hardware. It is calculated in terms of cost which depend on number of states and number of resources. The said metric defines the complexity of finite state machine and also its performance. The control logic size and delay is generally ignored which results in inaccurate estimation[1-4]. If estimation done in High level synthesis is inefficient, final hardware implementation will be inefficient, So it is a must that optimization should be carried out in High level synthesis. Normally behavioral hardware description language specification is mapped into a register transfer level is known to be the process for High Level Synthesis[5-9].

The behavioral description is converted into intermediate format, the format can be Control flow graph(CFG), Data Flow Graph(DFG), Control Data Flow

Graph(CDFG), Finite state machine (FSM), and Codesign finite state machine (CFSM). The internal representation is completely different from final hardware that is estimated. Though CDFG has hardware resource in its nodes, it does not have control logic implementation. The value is represented as register or net in hardware based on the schedule[10-14]. The hardware resources when implemented is realized with surrounding logic. So it will be inaccurate when hardware operators adder/subtractor alone is considered as a hardware. Actual estimation cannot be done after high level synthesis or logic synthesis. Estimation is carried out closer to language level than hardware level. High level synthesis and logic synthesis operate with different intermediate format results with inefficient estimation. This problem can be avoided by using same intermediate format in both the domain. Behavioral Network Graph (BNG) is used to represent from intermediate representation (CDFG) which is equivalent to unscheduled behavioral descriptions. States are determined based on the hardware resources. RTL network depends on the states which is registers[15-19]. States are not known in prior in the behavioral description. Unscheduled graph represents multiple RTL networks. The adders are placed in the unscheduled Behavioral network graph which represents all possible schedules [20-24].

This paper is organized as follows. Section II presents High level Synthesis. Section III explains the algorithms for BNG generation. Section III presents the conclusion[25-27].

2. High Level Synthesis

The behavioral description is transformed into intermediate representation (CDFG). The generated CDFG is undertaken for compiler optimization like constant propagation, loop unrolling and data flow analysis. High level synthesis system have language parser to create the intermediate format and which is then taken for optimization. Finite state machine is generated from scheduled task graph, a datapath is created by allocation and resource sharing both are combined for an

RTL network. CDFG is taken for parallelism extraction and equivalent BNG representation is obtained. Scheduling, allocation and resource sharing are performed on the BNG. The cost involved is calculated and its RTL/Gate level network is obtained [28-30]

2.1 Control Data Flow Graph

The Control Data Flow graph represents the control construct and data dependencies. A separate Control Flow Graph and Data Flow Graph may also be represented for entire language specification. HDL language is transformed into CDFG. The life time of each variable is calculated and scheduled accordingly. Traditional algorithms like list scheduling and force directed scheduling explores parallelism in the data path does not handle well on control construct. Path based Scheduling and Symbolic scheduling to interact between control and data.

2.2 Behavioral Network Graph

FSM for all possible schedules is generated from Control Flow Graph. State cuts are placed based on the number of hardware operation available. State value node is used represent each node. The hardware generated from BNG uses one hot encoded FSM. State cut can be placed in any CFG edge. A Simple control data flow graph is taken as shown in Figure 1. Each edge is named with state cut variable SC_i . The node associated with hardware operations are also shown.

Each node is replaced by state value node. The state value node is replaced either as wire or a register as shown in Fig 2. Basically state value comprises of register and multiplexer which is realized either as wire or multiplexer. To estimate number of AND gate and OR gate to realized as final RTL/gate level network, a simple matrix method is used. Each node and its successor is plotted as a matrix as shown in Table 1.

Table 1.Matrix Representation

	0	1	2	3	4	5	6	7	8	9	10
0		1									
1			1								
2				1				1			
3					1						

4						1					
5							1				
6									1		
7								1			
8										1	
9											1
10	1										

The number of 1's in each row is checked if more than one 1, it is replaced with AND gate and if there n 1's in the column its succeeding column is increased (n-1) times and replaced with OR gate. An estimation for AND gate and OR gate is done in matrix method. The steps for generating the Behavioral Network Graph is discussed.

STEP 1: CFG is traversed and place SC_i variable in each node.

Variables SC_{ia} , SC_{ib} ,... are associated with each predecessor edge If a node has multiple predecessors.

STEP 2: Node with single predecessor and single successor is identified and replaced with state value node STN_i .

STEP 3: For join nodes, a state value node STN_{ij} is created for each predecessor edge and all STN_{ij} nets are connected to a single OR gate. The output of the OR gate is called net STN_i .

STEP 4: For Fork nodes i.e. multiple successor edges STN_i is created and connected to one of the input of AND gates as successor edges. Two input AND gate is used. The first input is net STN_i (for the fork node) and the other input is a net representing the corresponding successor edge.

STEP 5: Connect the multiple STN_i boxes as the CFG. Equivalent BNG as per the above steps are generated and shown in Fig 3. Hardware operators are highlighted in the Fig 3. The state cut $SC_1=1$, $SC_2=1$, $SC_4=1$, $SC_5=1$ are assigned for one hardware availability. The equivalent hardware generated for provided state cut is shown in the Fig 4.

Theoretically FSM is generated for the graph with state cut. We have implemented the Hardware estimator and

checked for different control construct. The FSM for the graph with state cut is represented in the Fig 5.

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the state cut should be one at 37b
***** STEP 3 *****
The CONTROL BNG is
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3<-1&a=0
13a<-3
5<-1&b=1
13b<-5
7<-1&b=0
8<-7
13c<-8
10<-1&b=1
11<-10
12<-11
13d<-12
15<-13a+13b+13c+13d
15<-13a+13b+13c+13d
15<-13a+13b+13c+13d
15<-13a+13b+13c+13d
16<-15
17<-16
19<-17&c=0
31a<-19
21<-17&c=1
22<-21
31b<-22
24<-17&d=0
25<-24
26<-25
31c<-26
28<-17&d=1
29<-28
30<-29
31d<-30
33<-31a+31b+31c+31d
33<-31a+31b+31c+31d
33<-31a+31b+31c+31d
33<-31a+31b+31c+31d
34<-33
36<-34&b=0
37b<-36

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Figure 1.Generate Control BNG

3. Conclusion

An elliptic filter is estimated using this tool. The estimated output for filter is shown in the fig 6. The control construct is given as an input and also the hardware resources with its node and conditions. Based on availability of hardware the tool generates state cut and provides the control BNG which shows how many registers, AND gate and OR gate is required for control construct .

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