

DIGITAL PHASE LOCKED LOOP

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Abstract: The wide range advanced phase locked loop(PLL) utilizing self redressing DCO is intended to enhance the recurrence go when contrasted with the past strategies. It likewise diminishes the power utilization and defer when contrasted with the past techniques. It gives great setup that meets the client characterized necessity as well as accomplishes a littler zone and lower control utilization than a run of the mill manual plan. The silicon estimation comes about demonstrate this is without a doubt a promising new option for simple phase locked loops, particularly for cutting edge nanometre innovations. Generally, the PLL is made out of some simple pieces, e.g., charge pump and voltage-controlled oscillator (VCO). The simple flags in these simple squares have a tendency to be powerless to the clamour caused by the oftentimes exchanging of the advanced signs. Moreover, the power dissipation issue will turn out to be progressively genuine in cutting edge CMOS forms. Thus, the trouble and the intricacy of outlining a simple PLL increment as the innovation procedure propel. In this manner, there are increasingly looks into concentrating on the all digital stage bolted circle.

1. Introduction

Phase Locked Loops (PLLs) are one of the essential building hinders in present day electronic frameworks. They have been generally utilized as a part of interchanges, media and numerous different applications[1-3]. The hypothesis and scientific models used to portray PLLs are of two sorts: direct and nonlinear. Nonlinear hypothesis is regularly confused and hard to manage in genuine plans. Simple PLLs have been all around displayed by direct control hypothesis[4-6]. It has been demonstrated that a straight model is sufficiently exact for most electronic applications as long as specific conditions are met. A phase locked loop (PLL) is a control framework that produces a yield flag whose stage is identified with the period of an information flag. While there are a few contrasting sorts, it is anything but difficult to at first imagine as an electronic circuit comprising of a variable oscillator and a stage finder. The oscillator

produces an intermittent flag[7-11]. The stage finder contrasts the period of that flag and the period of the information intermittent flag and changes the oscillator to keep the stages coordinated.

A. Existing System

The block diagram for the existing digital phase locked loop is as follows .

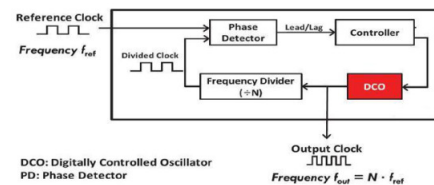


Figure 1. Existing system

It consists of four major blocks are a phase detector, an ADPLL controller, a programmable frequency divider and one DCO. The phase detector is to compare the phase polarity between the divided-clock signal and the reference clock signal[22-26]. It generates two mutually exclusive signals: lead and lag, to show whose edge is leading.

B. Proposed System

The block diagram for our proposed system is as follows

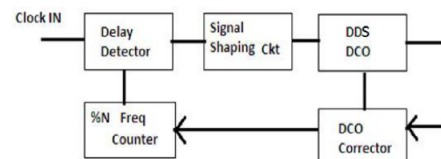


Figure 2. Proposed system

In the proposed design we are planning to implement the digital PLL technique with self correcting DCO. We designed this all digital phase locked loop used to generate various wide range of frequencies. We designed this ADPLL using phase detector, loop filter, DDS DCO, DCO corrector and frequency counter. In the digital phase locked loop we generate the clock signal it will give wide range frequency up to 5GHZ. In the proposed system we have used a signal shaping circuit instead of loop filter and we have implemented self correcting technique in DCO

i. Module 1: Design Of Delay Detector

This module consists of d flip flop and logic gates. In the proposed phase locked loop delay detector act as phase generator. It generates the UP frequency, DOWN frequency and the phase. Clock is the input for this module. Delay detector as the name suggests it determines the delay between the input clock signal and the reference clock signal. In the previous methods phase detector is usually designed with the help of XOR gates but in our proposed system we have implemented it using Flip-flops and NAND gates.

ii. Module 2: Design Of Signal Shaping Circuit

Signal shaping circuit is designed with the help of up counter and down counter. Previous delay detector frequency is the input for this module. The UP signal or DOWN signal from the delay detector is given to the signal shaping circuit and the output is either CARRY or BORROW which is then given to the DCO

iii. Module 3: Design Of Self Correcting Dco

Digital Control Oscillator designed by the t flip flop and logic gates. It generates some clock signal in constant frequency. The DCO either oscillates in high frequency or low frequency depending on the input given to it. Either CARRY or BORROW is given as the input to the DCO. The DCO tunes the input clock signal as close as possible to the reference signal. The self correcting block is to further decrease the delay in the tuned signal. The self correcting block again compares the reference clock signal and the DCO output and checks for any delay in the output.

iv. Module 3: Design Of Reference Generation

This module consists of all kinds of reference signals generations, reference pulses generation and control pulse generation etc which is used for triggering the modules (Which act as a state machine). It generates the various frequency clock signals. The reference generator block is an internal block. This block is used to generate reference clock signals as per the user requirements. The reference signal is generated as an internal clock by giving selection lines as the input

2. Literature Survey

Parameterised all digital PLL architecture and its compiler to support easy process migration, Chao-Wen Tzeng, Shi-Yu Huang (IEEE Transaction on VLSI march 2014) [1]. In this paper Digital pll using delay detector and DCO and a programmable frequency divider is designed($0.18 \mu\text{m CMOS}$). The advantages in this paper are Low power consumption (7.2 mw @ 1000 MHZ) and Low jitter (4.3 ps). The limitations in this paper are Frequency range is 1 GHZ which is low when compared to the proposed system A low power

Digitally controlled oscillator for Digital PLL, Jun Zhao and Yong-Bin Kim (Open journal under creative common attributions october 2009) [2]. In this paper a 12 bit CMOS DCO implemented with schmitt trigger inverter (32 nm CMOS predictive technology model). The advantages in this paper is that Power consumption is low (2.2 mw @650 MHZ) and limitations is that High jitter when compared to proposed system(67 ps) and Low frequency Range (650 MHZ) An Ultra-Low-Power 15-bit Digitally Controlled Oscillator with High Resolution, Nasser Erfani Majd and Mojtaba Lotfizad (Scholar link Research Institute Journals, 2011) [3]. 15 bit DCO designed based on segmental coarsetuning stage and employed by hysteresis delay cell. The advantage in this paper is that Power consumption is very low in the range of micro watts ($225 \mu\text{W}$ @205 MHZ) and the limitations are Frequency range is very low (205 MHZ) and Jitter is high it is in the range of 90 ps. An all Digital Phase Locked Loop for high speed clock generation, Ching Che Chung and Chen Yi Lee (IEEE journal For solid state circuits february 2001[4]. In this paper PLL is implemented using Implemented using standard cells in $0.35 \mu\text{m CMOS}$. The advantage in this paper is High speed clock generation and Jitter is low (39 ps). The limitation in this paper is that Frequency Range is low (400 MHZ-500 MHZ).

3. Construction And Working

A. Delay Detector

The delay detector in the designed phase locked loop is nothing but an phase detector. The delay detector as the name suggests determines the delay between the input frequency and the reference frequency. In the previous methods phase detector is designed with the help of XOR gates but in our design we have implemented the same operation with the help of D flip flops and universal NAND gates. The circuit diagram for Proposed delay detector is as

follows

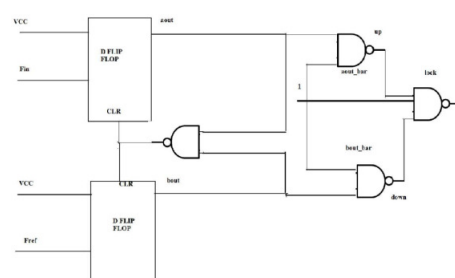


Figure 3. Delay detector

As you can see from the circuit diagram instead of using different logic gates we have implemented the same process with the help of only NAND gates in order to simplify the circuit of the delay detector We have implemented the operation of AND,OR and XOR with the

help of combination of NAND gates. As the circuit diagram suggests the delay detector consists of two D flip flops. The input of one flip flop is the input frequency and the input to the second flip flop is the reference frequency. The input V_{cc} is given as 1 and for the first cycle the clear is zero so the output of the flip flops are also zero then for the next cycle the output of the flip flops are NAND and given as clear input hence for the second cycle the clear is one and hence the D flip flop activates in the second cycle. If the reference frequency leads the input frequency then the UP signal is generated by the delay detector and if the reference frequency lags the input frequency then the DOWN signal is generated. The UP and DOWN signal is nothing but the difference between the rising edges of the reference and input frequencies. The UP and DOWN signal are given as input to an NAND gate and the output of the NAND gate is the output of the delay detector.

B. Signal Shaping Circuit

The signal shaping circuit in our proposed technique is planned with an up counter and a down counter. In the past techniques circle channel is utilized rather than signal shaping circuit. The circle channel dispenses with the undesirable frequencies from the postpone locator yield while the signal shaping circuit takes out the undesirable frequencies and furthermore shapes the yield flag. The block diagram for the signal shaping circuit is as follows.

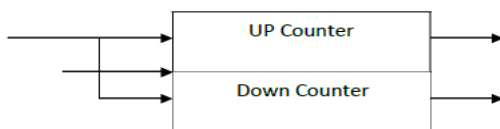


Figure 4. Signal shaping circuit

The UP signal or DOWN signal from the delay detector is given as the input to the signal shaping circuit. If the UP signal is produced then it is given to the up counter else if DOWN signal is produced then it is given to the down counter. If the up counter works then CARRY is obtained as the output of the signal shaping circuit else if the down counter works then BORROW is obtained as the output of the signal shaping circuit.

C. Digitally Controlled Oscillator

Digitally controlled oscillator is used instead of voltage control oscillator to overcome the tuning stability limitations of voltage control oscillator. A DCO can be considered as a VCO that is synchronised to an external frequency reference. The reference in this case is the reset pulses. These pulses are produced by a digital counter. The counter acts as a frequency divider, counting pulses from a high frequency master

clock (typically several MHz) and toggling the state of its output when the count reaches some predetermined value. The frequency of the counter's output can thus be defined by the number of pulses counted, and this generates a square wave at the required frequency. The leading edge of this square wave is used to derive a reset pulse to discharge the capacitor in the oscillator's ramp core. This ensures that the ramp waveform produced is of the same frequency as the counter output. Hence the digitally controlled oscillator tunes the input frequency as close as possible to the reference frequency. The circuit diagram for the proposed digitally controlled oscillator is as follows.

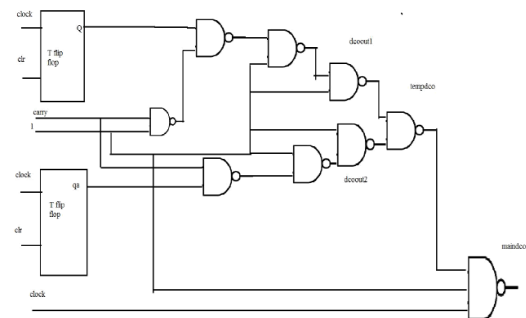


Figure 5. Digitally controlled oscillator

The output from the signal shaping circuit is given to the digitally controlled oscillator as the input to the DCO. The digitally controlled oscillator in the proposed system is designed with the help of toggle flip flops and universal NAND gates. Inverted input is given to one NAND gate and the non inverted input is given to other NAND gate. The output of the DCO is considered as the temporary output which is then given to the DCO corrector block. The DCO correction is nothing but comparing the tuned signal to the reference signal to determine the delay in the tuned signal. If any delay is found then the DCO tunes the signal to decrease the delay as low as possible. The tuning range of the proposed DCO is very high when compared to the previous methodologies. If the carry is given as the input to the DCO then the DCO increments the input frequency until it is in phase with the reference frequency. If the borrow is given as the input to the DCO then the DCO decrements the input frequency until it is in phase with the reference frequency.

D. Frequency Divider

Digital PLL's include frequency counter between the reference clock and the reference input to the delay detector to produce a frequency synthesizer. If the frequency counter in the feedback path divides by integer, it allows the PLL to multiply the reference frequency. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be changed by other issues, and then the reference frequency from frequency counter is useful. Frequency divider is used to generate various reference frequencies applied to the delay detector to compare with the input frequency signal. Frequency multiplication can also be

attained by locking the DCO output to the n th harmonic of the reference signal. The DCO output is tuned near to the input frequency. The input to the frequency divider is given as selection lines. In the program we have done up to twenty counts that is zero to nineteen. when the selection line input changes then reference frequency changes accordingly and hence the output of the PLL also changes. In our proposed PLL we have obtained frequency range up to 5 GHZ.

4. Experimental Results

A. Delay Detector

SIMULATION RESULT – $F_{in} < F_{ref}$

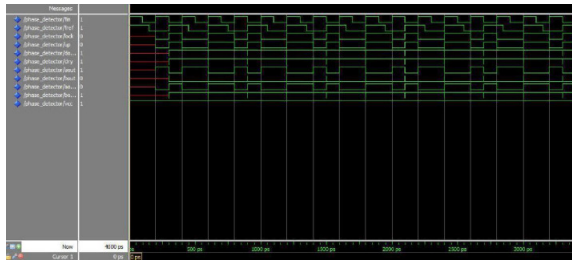


Figure 6. Delay detector $F_{in} < F_{ref}$ simulation

SIMULATION RESULT – $F_{in} = F_{ref}$

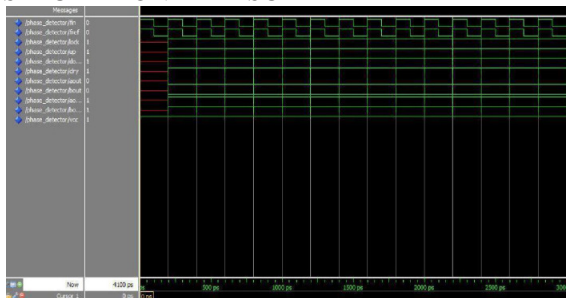


Figure 7. Delay detector $F_{in} = F_{ref}$ simulation

SIMULATION RESULT – $F_{in} > F_{ref}$

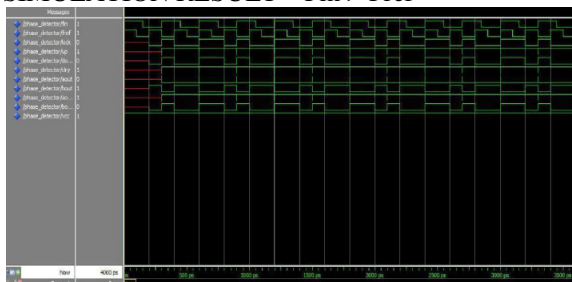


Figure 8. Delay detector $F_{in} > F_{ref}$ simulation

B. Signal Shaping Circuit

If UP signal is generated

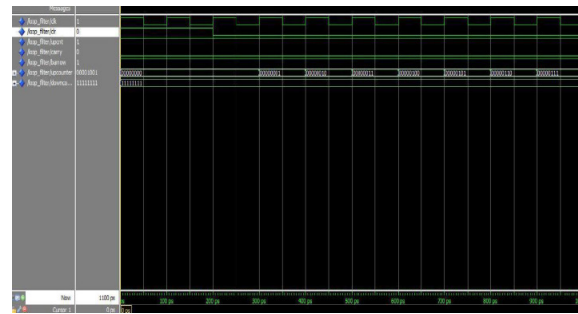


Figure 9. Signal shaping circuit UP simulation
If DOWN signal is generated

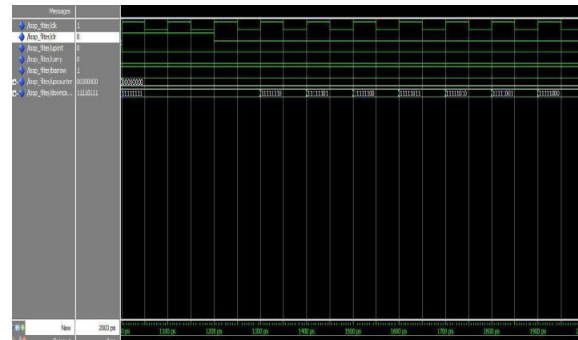


Figure 10. Signal shaping circuit DOWN simulation

C. DIGITALLY CONTROLLED OSCILLATOR

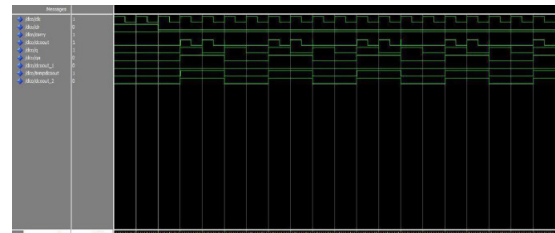


Figure 11. Digitally controlled oscillator simulation

D. REFERENCE GENERATOR

For selection line – 00000001 Frequency = 5GHZ

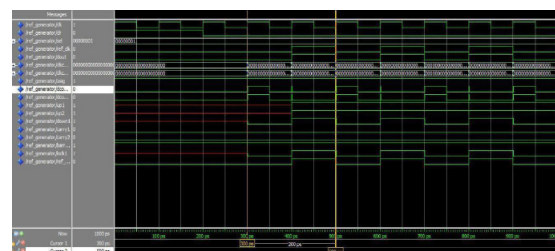


Figure 12. Reference generator 5 GHZ simulation
For selection line – 00000010 Frequency = 2.5 GHZ

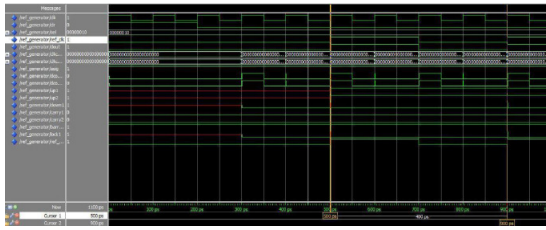


Figure 13. Reference generator 2.5 GHz simulation
For selection line – 00000011 Frequency = 1.25 GHz

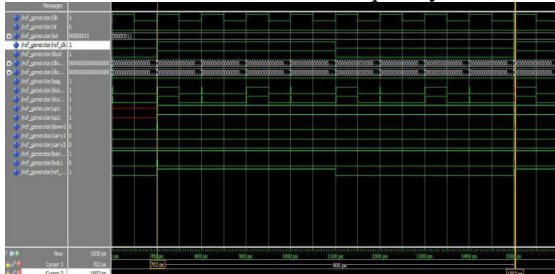


Figure 14. Reference generator 1.25 GHz simulation
Thus the frequency keeps on decreasing as the selection line count increases and various ranges of frequency is generated with the highest being 5 GHz.

Xilinx Report

A. Filter Report

Design Name	ref_generator
Fitting Status	Successful
Software Version	L.33
Device Used	XC9572XL-5-PC44
Date	4- 2-2015, 2:41PM

Resource Summary

Macrocells Used	Pterms Used	Registers Used	Pins Used	Function Block Inputs Used
24/72 (34%)	72/360 (20%)	22/72 (31%)	12/34 (36%)	79/216 (37%)

Pin Resources

Signal Type	Required	Mapped	Pin Type	Used	Total
Input	8	8	I/O	9	29
Output	2	2	GCK/IO	1	3
Bidirectional	0	0	GTS/IO	1	2
GCK	1	1	GSR/IO	1	1
GTS	0	0			
GSR	1	1			

Global Resources

Signal mapped onto global clock net (GCK1)	clk
Signal mapped onto global output enable net (GSR)	clr

Power Data

Table 1. Filter Report

Macrocells in high performance mode (MCHP)	24
Macrocells in low power mode (MCLP)	0
Total macrocells used (MC)	24

B. Timing Report

Design Name	ref_generator
Device, Speed (SpeedFile Version)	XC9572XL, -5 (3.0)
Date Created	Thu Apr 02 14:42:01 2015
Created By	Timing Report Generator: version L.33
Copyright	Copyright (c) 1995-2009 Xilinx, Inc. All rights reserved.

Performance Summary

Table 6.2. Timing Report

Min. Clock Period	9.700 ns.
Max. Clock Frequency (fSYSTEM)	103.093 MHz.
Limited by Cycle Time for clk	
Clock to Setup (tCYC)	9.700 ns.
Setup to Clock at the Pad (tSU)	8.100 ns.
Clock Pad to Output Pad Delay (tCO)	3.500 ns.

5. Conclusion

Along these lines in the proposed framework we have actualized a phase locked loop utilizing self remedying DCO to create recurrence extends up to 5 GHz. We have just executed recurrence divider we have not gone for the recurrence multiplier since high frequencies can be unsafe though in our undertaking we have just utilized high recurrence motions as inward clock signals. Advance change in this paper is to apply phase locked for simple flags by utilizing simple to computerized converter.

Future Work

The proposed technique utilizes computerized contributions to phase secure in the coveted recurrence go. By utilizing simple flags, the phase locked loop can be connected to the continuous applications like simple correspondence and remote interchanges. The recurrence range can be expanded by utilizing number of bits utilized as a part of choice line utilized as a part of advanced controlled oscillator.

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