

DESIGN AND IMPLEMENTATION OF FAST MULTIPLIER USING MODIFIED CARRY SAVE ADDER

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Abstract: Arithmetic and Logic Unit (ALU), when used for scientific computations, will spend more time in multiplications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. Reducing delay in the multiplier reduces the overall computation time. Wallace multipliers perform in parallel, resulting in high speed. It uses full adders and half adders in their reduction phase. Reduced Complexity Wallace multiplier will have fewer adders than normal Wallace multiplier. A new multiplier is proposed with fast adders at the final stage of Wallace multipliers to reduce the delay. The presence of larger carry propagating adder indicates that wallace multiplier as faster multiplier. The fast adder (Modified carry save adder) is used at the final stage of the Wallace multipliers in order to reduce the delay.

Keywords: Parallel prefix adder, Carry save adder, Wallace multiplier, Modified carry save adder, High speed adder.

1. Introduction

The Multiplier is one of the key hardware blocks in most of the digital and high performance systems such as digital signal processors and microprocessors. The Wallace Tree basically multiplies two unsigned integers.

Design of high speed data path logic systems are one of the most substantial research area in VLSI system design. High speed addition and multiplication has always been a fundamental requirement of high performance processors and systems[1-5]. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The basic idea of the proposed work is using n-bit binary to excess 1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. The proposed 16, 32 and 64-bit adders are compared in this paper with the conventional fast adders such as carry save adder (CSA) and carry look ahead adder (CLA). This paper has realized the improved performance of the CSA with BEC logic through custom design and layout. The final stage CPA constitutes a dominant component

of the delay in the parallel multiplier [6]-[12]. Therefore decrease in carry propagation delay will result in major enhancement of the speed of the adder and multiplier [13-18].

2. Literature Review

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Power refers to number of Joules dissipated over a certain amount of time whereas energy is the measure of the total number of Joules dissipated by a circuit. The performances of the exiting multiplier schemes are limited by the time to do a carry propagate addition. Carry propagate adds are relatively slow, because of the long wires needed to propagate carries from low order bits to high order bits[19-23]. Probably the single most important advance in improving the speed of multipliers, pioneered by Wallace, is the use of carry save adders to add three or more numbers in a redundant and carry propagate free manner. By applying the basic three input adder in a recursive manner, any number of partial products can be added and reduced to two numbers without a carry propagate adder. A single carry propagate addition is only needed in the final step to reduce the two numbers to a single final product[24-30].

3. Conventional Method

A. Wallace Tree Multiplier

The partial products are formed by N2 AND gates. For the conventional Wallace reduction method, once the partial product array (N2 bits) is formed, adjacent rows are collected into non-overlapping groups of three. Each group of three rows is reduced by

- Applying a full adder to each column that contains three Bits.
- Applying a half adder to each column that contains two bits, and

- Passing any single bit columns to the next stage without processing

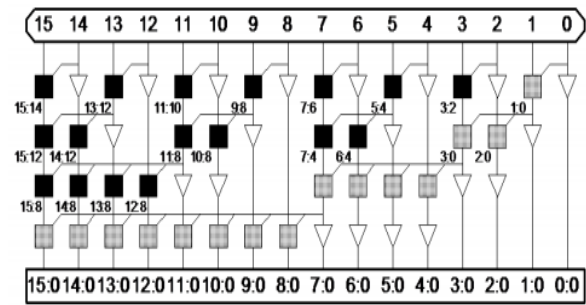
This reduction method is illustrated by the conventional 8-bit Wallace multiplier. The reduction is performed in four stages (each with the delay of one full adder). The third phase will require a $(2N-1-S)$ wide adder, where S – number of stages in reduction.

- Optimized column adder tree
- Combines all partial products into 2 vectors (carry and sum)
- Carry and sum outputs combined using a conventional adder
- Delay is $\log(n)$
- Wallace tree multiplier uses Wallace tree to combine $1 \times n$ partial products
- Irregular routing
- Not optimum in many FPGAs

A Wallace tree is an implementation of an adder tree designed for minimum propagation delay. Rather than completely adding the partial products in pairs like the ripple adder tree does, the Wallace tree sums up all the bits of the same weights in a merged tree. Usually full adders are used, so that 3 equally weighted bits are combined to produce two bits: one (the carry) with weight of $n+1$ and the other (the sum) with weight n . Each layer of the tree therefore reduces the number of vectors by a factor of 3:2 (Another popular scheme obtains a 4:2 reduction using a different adder style that adds little delay in an ASIC implementation). The tree has as many layers as is necessary to reduce the number of vectors to two (a carry and a sum). A conventional adder is used to combine these to obtain the final product. The structure of the tree is shown below.

B. Sklansky Adder

The Sklansky or divide-and-conquer tree on reduces the delay to $\log 2N$ stages by computing intermediate prefixes along with the large group prefixes. This comes at the expense of fan-outs that double at each level: The gates fanout to $[8,4,2, 1]$ other columns. These high fan-outs cause poor performance on wide adders unless the gates are appropriately sized or the critical signals are buffered before being used for the intermediate prefixes. Transistor sizing can cut into the regularity of the layout because multiple sizes of each cell are required, although the larger gates can spread into adjacent columns. With appropriate buffering, the fan-outs can be reduced to $[8,1,1,1]$. The goal of this project is to realize 16bit Sklansky adder by using static CMOS devices. Sklansky adder belongs to tree adder family. The difference between Sklansky adder and other tree adders is prefix network. Compare to other tree adders, Sklansky adder has minimum logic levels, wiring tracks, but maximum fanout. Also, it has largest delay at the same condition.



This is one type of adder. It is used to find a sum and carry of binary inputs. This adder is also called as conditional adder. The Sklansky adder is proposed in the year of 1960. It is invented by the inventor J. SKALANSKY. The Sklansky adder has Minimal depth and High fanout.

C. Kogge Stone Adder

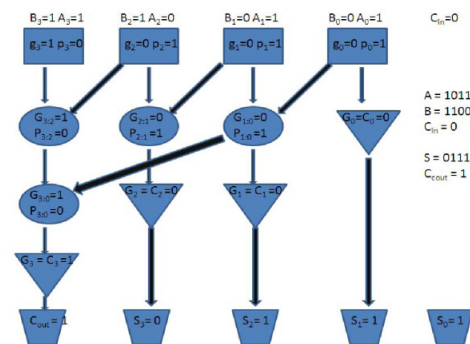


Figure 2. Illustration of 4 bit KSA

The complete functioning of KSA can be comprehended by analyzing it in terms of three distinct parts :

1) *Pre processing*: This step involves computation of generate and propagate signals corresponding to each pair of bits in A and B. These signals are given by the logic equations below:

$$p_i = A_i \text{ xor } B_i$$

$$g_i = A_i \text{ and } B_i$$

2) *Carry look ahead network*: This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic equations below:

$$P_{i:j} = P_{i:k+1} \text{ and } P_{k:j}$$

$$G_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j})$$

3) *Post processing*: This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits. Sum bits are computed by the logic given below:

$$S_i = p_i \text{ xor } C_{i-1}$$

4. Proposed Method

D. Reduced complexity Wallace Tree Multiplier

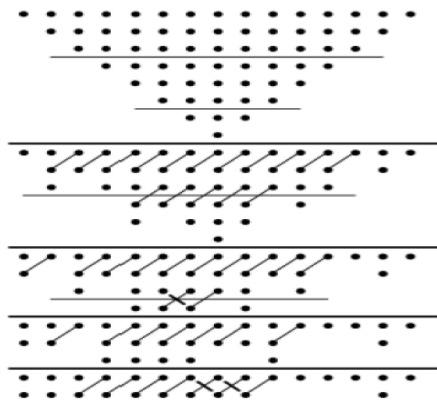


Figure 3. Reduced complexity Wallace tree multiplier:

Reduced Complexity Wallace tree reduces the number of partial products to be added into 2 final intermediate results. Wallace tree basically multiplies two unsigned integers. Three stages of Reduced Wallace tree Multiplier are

- Partial Product Generation Stage
- Partial Product Reduction Stage
- Partial Product Addition Stage

Partial product generation stage is obtained using AND array, partial product reduction is accomplished by the use of Reduced complexity Wallace multiplier and the final stage of addition is performed by modified carry save adder. It is the modified version of Wallace tree multiplier it has less half adder than the normal Wallace multiplier. The partial products are formed by N^2 AND gates. The partial products are arranged in an "Inverted triangle" order. The modified Wallace reduction method divides the matrix into three row groups.

- Use full adders for each group of three bits in a column like the conventional Wallace reduction.
- A group of two bits in a column is not processed, that is, it is passed on to the next stage (in contrast to conventional method). Single bits are passed on to the next stage as in the conventional Wallace reduction.
- The only time half adders are used is to ensure that the number of stages does not exceed that of a conventional Wallace multiplier. For some

cases, half adders are only used in the final stage of reduction.

E. Modified Carry Save Adder

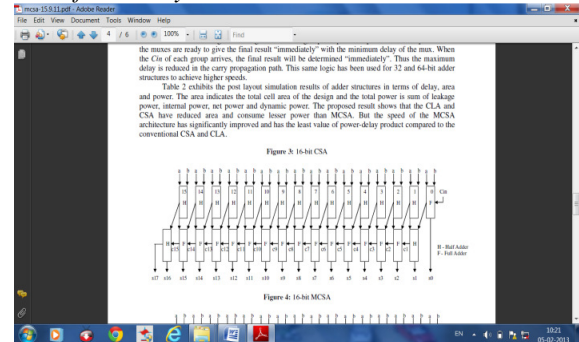


Figure 4. 16 bit carry save adder

The 16-bit conventional CSA is shown in Figure 3. It has 17-half adders and 15-full adders. Since the ripple carry adder (RCA) is used in the final stage, To reduce this delay, the final stage of CSA is divided into 5 groups as shown in Figure 4. The first group includes $1 + \log_2 n$ -bit value and other groups includes $n/2 \log$ -bit value, where n is the bit size of the adder. The divided groups are listed below,

- $\{c_4, s[4:0]\}$
- $\{c_7, x[7:5]\}$
- $\{c_{10}, x[10:8]\}$
- $\{c_{13}, x[13:11]\}$
- $x[17:14]$

The first group of output $s[4:0]$ are directly assigned as the final output; the second group $\{c_7, x[7:5]\}$ manipulates the partial result by considering c_4 is 0; the third group $\{c_{10}, x[10:8]\}$ manipulates the partial result by considering c_7 is 0; the fourth group $\{c_{13}, x[13:11]\}$ manipulates the ASIC

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H - Half Adder

F - Full Adder

partial result by considering c_{10} is 0 and the fifth group $x[17:14]$ manipulates the partial result by considering c_{13} is 0.

Depending on c_4 of the first group, the second group mux gives the final result without the carry propagation delay from c_4 to c_7 ; depending on c_7 of the second group final result, the third group mux gives the final result without the carry propagation delay from c_7 to c_{10} ; depending on c_{10} of the third group final result, the fourth group mux gives the final result without the carry propagation delay from c_{10} to c_{13} and depending on c_{13} of the fourth group final result, the fifth group mux gives the final result without the carry propagation delay from c_{13} to $s[17]$. The main advantage of this logic is that each group computes the partial results in parallel and the muxes are ready to give the final result "immediately" with

the minimum delay of the mux. When the *Cin* of each group arrives, the final result will be determined “immediately”. Thus the maximum delay is reduced in the carry propagation path. This same logic has been used for 32 and 64-bit adder structures to achieve higher speeds. Table 2 exhibits the post layout simulation results of adder structures in terms of delay, area and power. The area indicates the total cell area of the design and the total power is sum of leakage power, internal power, net power and dynamic power. The proposed result shows that the CLA and CSA have reduced area and consume lesser power than MCSA. But the speed of the MCSA architecture has significantly improved and has the least value of power-delay product compared to the conventional CSA and CLA. Pipelining operation is used to obtain the final multiplier output.

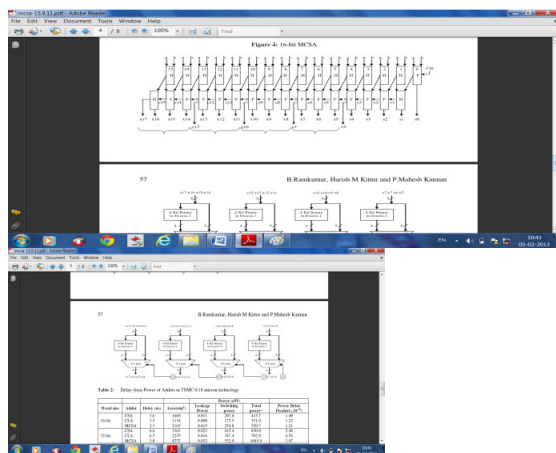


Figure 5. 16 bit modified carry save adder

IV. RESULT AND DISCUSSION

In this section, the proposed and the conventional architectures have been compared. Implementation of 8-bit multiplication using Reduced complexity Wallace tree multiplier and parallel prefix adder such as modified carry save adder has been simulated in ModelSim 6.2 tool and synthesised using Xilinx ISE 9.1. The speed and power result of adders and multiplier circuit are improved in the proposed system compared to conventional system.

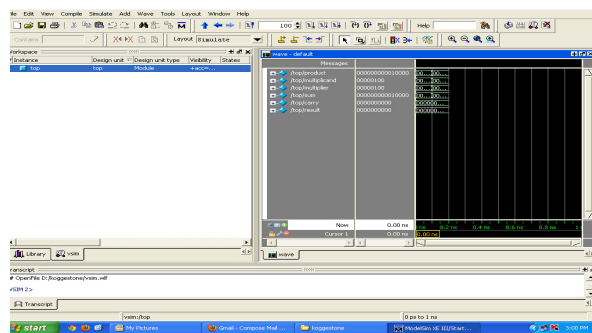


Figure 6. Simulation result of proposed multiplier circuit

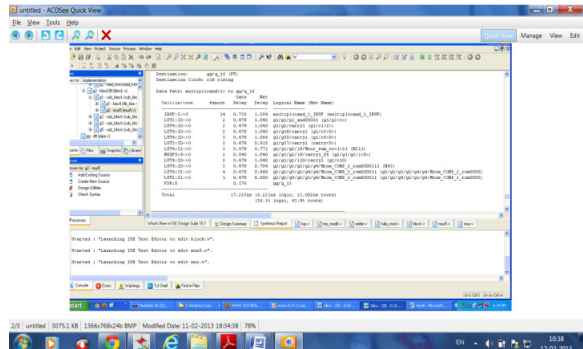


Figure 7. Synthesis result of proposed multiplier circuit

5. Conclusion

The time taken for multiplication operation is reduced by employing the wallace multiplier. Here integrated reduced wallace multiplier architecture is proposed for further reduction in time. This architecture has been chosen keeping low power as main objective. BEC logic can be used with any type of adder to enhance the speed of addition. The MCSA are faster and very suitable for VLSI hardware implementation, than the other known architectures.

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