CNTFETS AND RECONFIGURABLE GATE ARRAYS: A REVIEW

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Abstract

Carbon Nanotube Field Effect Transistors (CNTFETs) offer 1-D ballistic transport of electron/holes from source to drain and also offer very high ON current and high transconductance. FPGAs are fault-tolerant devices due to their reconfigurable ability. The CNTFETs can be manufactured for creating repetitive regular structures, like in FPGAs. The programmability of the FPGA allows reconfiguration of the Logic Elements in the presence of large number of fabrication defects providing highest level of fault tolerance for nano-circuit operation. It is reported that the FPGAs designed with CNTFETs can withstand up to 30% metallic CNTs in semiconducting CNTs. In this paper, we review different CLB and routing architectures of FPGA to design a CNTFET based FPGA. Hybrid architectures with MUX:LUT ratio of 1:9 is found to have better 102.70% utilization of CLB.

Key Words and Phrases: CNTFET, FPGA, Fault Tolerance, CLB, DG-CNTFET, Reconfigurability
1 Introduction

The MOSFET devices at 22nm and below experience problems due to short channel effects and manufacturing processes. However, the short channel issues have been addressed by various techniques [1]. When the technology node is at 7nm and below, the gate loses its control over the channel. To overcome these problems multi-gate devices like FINFET and Gate All Around FET are used.

The Carbon Nanotubes (CNTs) are considered a potential replacement for Silicon [2]. The CNTs can be single-walled (SWCNT) or multi-walled (MWCNT) and they vary in their conductive properties. Chirality of CNTs determine whether it is metallic or semiconducting. CNTFETs are MOSFET-like devices which exploit semiconducting property of CNTs, offer 1-D ballistic transport of electrons and holes, high current and high transconductance [3].

FPGAs are known for its reconfigurability, rapid prototyping and fault-tolerant design. It has a longer lifetime, they are mapped to reduce strain [4]. Its fault-tolerant property ensures correct operation of nano-circuit while CNTFET offers very low delay and high packaging density. The CNT in its metallic form can be used as interconnects in Nano-switch cross arrays [5].

In this paper, we discuss the Configurable Logic Block (CLB) and routing architecture of FPGA and techniques to improve them. In Section II, we discuss the structure of CNTs and its model as Transistors. The techniques to improve the performance of FPGA is studied in Section III. Section IV deals with low power architectures for CNT in FPGA.

2 CNTs and its Transistor Models

2.1 Properties of CNTs

The CNT were first synthesized by Sumio Iijima [6] in 1991. CNTs are cylinders, with diameters ranging from 0.6 nm to 3 nm rolled from graphene sheets. Depending on the chiral angle of the CNT, the bandgap of the CNT varies, thus leading to variations in the conductive property of the CNT. The chiral angle ($\theta$) [3] can be represented in terms of chiral vectors (n, m) as in Eq. 1,
\[ \theta = \tan^{-1}\left( \sqrt{\frac{3m}{2n+m}} \right) \] (1)

Around the circumference of the tube, based on the geometry of carbon bonds, there are two limiting cases - the armchair and zigzag structure [3]. The armchair structure is metallic in nature while the zigzag structure is semiconducting [3]. The threshold voltage \( V_{th} \) of CNT [7] is given by the Eq. 2,

\[ V_{th} = \frac{E_g}{\sqrt{2}} = 0.43 \] (2)

where the diameter \( d \) of the CNT is, \( d = 0.783\sqrt{n^2 + m^2 + nm} \)

### 2.2 Structure of CNTFET

CNTFETs are fabricated by using a single walled CNT as the channel between two electrodes, which works as the source and drain contacts of the FET as shown in Figure 1.

Some of the most important aspects of the CNTFET are ambipolarity, high \( I_{on}/I_{off} \), high transconductance, gate capacitance, fringing capacitance, cut-off frequency and intrinsic delay [3].

### 2.3 Other potential CNTFET Structures

The DG-CNTFETs [3] has a double gate structure which is used in controlling the polarity of the device. The DG-CNTFET is made of three different regions: source, inner part and drain. The in-field polarity control of DG-CNTFETs can be useful in designing pull-up and pull-down network with same size [8].

The T-Gate Aligned Nanotube RF Transistors [9], are self-aligned T-gate design to carbon nanotube array transistors. It has high transconductance \( (\approx 180 \mu A/\mu m) \) and low \( I_{on}/I_{off}(\approx 2) \) thus suitable for Analog and RF applications.
### 3 Optimisation of FPGA

#### 3.1 Architecture of CLB

The performance of the FPGA can be improved by modifying the architecture of the CLB. The CLBs are either designed with a LUTs or Universal Logic Gates (ULG). Changes in either in the architecture of LUT or in the architecture of ULG or a mixture of LUT and ULG increases performance of the FPGA [10]. The 6-input LUT is preferred as it offers lower critical path delay and occupy lesser die area [11].

The main drawback of using LUTs is that they are inefficient in implementing multiplexers as the select lines must also be given as the inputs to the LUT rather than the multiplexer itself. A hybrid architecture [12] with the combination of multiplexers and LUTs increases the utilization of CLBs effectively. The increase in utilization of the CLB resource is shown in Table 1 (assuming constant routing).

#### 3.2 Multi-valued Logic in FPGA

The use of multi-valued logic in FPGAs can also improve the performance of the FPGA considerably [13]. Multi-valued logic reduces the number of routing lines at the expense of some additional hardware (analog front-end). Multiple threshold values can easily be achieved in CNTs by varying the diameter of the CNT.

Table 2 shows the comparison between Ternary [13] and Quaternary [14] circuits. It is observed that Quaternary Logic provides low power, low delay and low energy when compared with Ternary circuits.

<table>
<thead>
<tr>
<th>Architecture (MUX:LUT)</th>
<th>1:9</th>
<th>2:8</th>
<th>3:7</th>
<th>4:6</th>
<th>5:5</th>
</tr>
</thead>
<tbody>
<tr>
<td>% Increase in CLB Utilization</td>
<td>102.70</td>
<td>105.60</td>
<td>108.60</td>
<td>111.90</td>
<td>115.30</td>
</tr>
</tbody>
</table>

Table 1: Percentage increase in CLB utilisation [12]
<table>
<thead>
<tr>
<th></th>
<th>Delay (ps)</th>
<th>Average Power (µW)</th>
<th>Energy (oJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ternary-NOT</td>
<td>16.579</td>
<td>1.9392</td>
<td>4.76</td>
</tr>
<tr>
<td>Ternary-NAND</td>
<td>20.931</td>
<td>2.2739</td>
<td>4.76</td>
</tr>
<tr>
<td>Ternary-NOR</td>
<td>19.807</td>
<td>1.8899</td>
<td>3.743</td>
</tr>
<tr>
<td>Quaternary-NOT</td>
<td>8.175</td>
<td>0.101</td>
<td>0.825</td>
</tr>
<tr>
<td>Quaternary-NAND</td>
<td>21.85</td>
<td>0.108</td>
<td>2.359</td>
</tr>
<tr>
<td>Quaternary-NOR</td>
<td>16.82</td>
<td>0.110</td>
<td>1.851</td>
</tr>
</tbody>
</table>

Table 2: Performance - Quaternary and Ternary circuits [13,14]

The CNTFETs can be manufactured in regular structures, making them ideal for creating repetitive architectures as found in the FPGAs.

The CNT based LUTs [15] are designed using parallel ribbons of SWCNTs held in place by metal electrodes and crossed by metal gates. Decoders are formed at CNTs and metal crossing points while NRAM is formed at points of CNT ribbons and substrate trenches.

The ULG based BLE offers very high reduction in area and delay. The DG-CNTFET with its in-field polarity control enables a reconfiguration of the circuit at the transistor level. The reconfigurable cell as shown in Figure 2 has higher degree of reconfigurability and also has reduced size when compared to its CMOS counterparts. The use of CMOS based ULGs instead of LUTs led to 54.74% reduction in area, 61.54% reduction in delay and 65.30% reduction in power consumption [16].

3.3 CNTFET in FPGA

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5
3.4 CNT - Routing in FPGA

CNTs can be used as interconnects as they provide very low contact resistances and low coupling capacitances. The SWCNT is preferred over MWCNT as SWCNT has higher performance than MWCNT[3]. However, MWCNTs can also be used in Power Local Interconnects by adding a catalyst to it. The Universal Switch Block Routing Architecture using FPGAs to achieve very high performance is proposed in [15]. The interconnects between the array of CNTs is provided using nano-switches in [10] a more efficient way is proposed to connect nanowires for routing through the logic blocks. Another efficient way to provide efficient switches between nanowires is by using the Field Programmable Nanowire Interconnects [5] which provides a rectangular array of identical cells, surrounded by periphery of I/O cell pairs.

3.5 Fault Tolerant CNTFET based FPGA Design

The CNTFETs circuits has not gained much popularity amongst designers as due to presence of metallic impurities in semiconducting CNTs. The programmability of the FPGA allows reconfiguration in presence of large number of fabrication defects, providing highest level of fault tolerance [17]. A fault simulation tool as proposed in [17] is designed to work with VPR, to provide investigation of metallic CNTs effect on CNTFET-based FPGAs. The CNTFET based FPGA with metallic CNT impurity of 30% offers a 1.13 times footprint reduction when compared with CMOS FPGA [17].

4 Low Power Design using CNT

When speed of the circuit is not the primary concern for operation, the device is designed to operate in sub-threshold region with sub-threshold leakage current as the operating current to achieve ultra-low power operation. As the threshold voltage is a function of diameter [7] and metal [3] used low power operation can be achieved using CNTs. Variation in diameter of CNT not only affects the threshold voltage of circuit but also parameters like transconductance, $I_{on}/I_{off}$ ratio, and saturation current value (Table 3)[7].
5 Conclusion

In this review paper, we discussed various CLB and routing architectures, multi-valued circuits, low power design and fault tolerance of FPGA. Of the architectures discussed above, the hybrid architectures (ULG:LUT) have better characteristics in terms of area, delay and power consumption. This is because of the 54.74%, 61.54% and 65.30% reduction in area, delay and power respectively in ULGs when compared to the LUTs. Though the multi-valued logic requires additional circuitry, overall reduction in area and power consumption can be achieved by minimising the routing overhead. Higher degree of reconfigurability in ULGs can be achieved by use of DG-CNTFETs. Fault tolerant property of FPGAs play a major role in reconfiguration of logic elements in the presence of large number of fabrication defects. In addition, CNT threshold level engineering is also studied for low power operation.

6 References


<table>
<thead>
<tr>
<th></th>
<th>D (nm)</th>
<th>L (nm)</th>
<th>Isat (µA)</th>
<th>gm (µS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>p-type I</td>
<td>1.7</td>
<td>50</td>
<td>25</td>
<td>30</td>
</tr>
<tr>
<td>p-type II</td>
<td>1.5</td>
<td>120</td>
<td>25</td>
<td>25</td>
</tr>
</tbody>
</table>

Table 3: Variation in Parameters w.r.t Diameter of CNT [7]


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