BALANCING OF DC LINK VOLTAGE USING THE PROPOSED REDUNDANT VECTOR ALGORITHM ASSOCIATED WITH SLIDING REGULATOR USED TO CONTROL THE SHUNT APF

Dr D SRINIVAS¹, PRATIMA DAS²,
Professor¹, Asst.Professor²,
DEPT OF EEE
MRIET, HYDERABAD, INDIA.
sudha.anisetti@gmail.com, daspratima45@gmail.com

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Abstract

In this paper, the control of DC interface capacitor voltages of 5-level diode clamped Active Power Filter (APF) utilizing improved Space Vector Pulse Width Modulation (SVPWM) related with the repetitive vectors of this topology is proposed. The space vector outline of the five-level inverter is disentangled into that of three-level inverter. Thusly, the three-level inverter space vector graph is rearranged into that of two-level inverter. In this way, the calculation of five-level SVPWM turns out to be fundamentally the same as that of ordinary two-level inverter SVPWM. Concerning the self adjustment of dc interface capacitor voltages, on the base of position of reference voltage vector in space vector outline, we disclose how to pick exchanging states that will be utilized to create the yield voltages. The redundancies
of some exchanging states are astutely used to wipe out unevenness of dc interface capacitor voltages, on the base of a shut circle that utilization estimations of info and yield streams of the APF. The execution of the proposed excess vector calculation related with sliding controller used to control the shunt APF is delineated through the remuneration of consonant streams and receptive power delivered by a non-direct load in medium voltage organize.

Key Words: Active Power Filter, Harmonic current, Five-level inverter, Space Vector Pulse Width Modulation (SVPWM), DC source balancing, Redundant vectors

1 INTRODUCTION

The use of energy gadgets, for example, circular segment heaters, flexible speed drives, PC control supplies and so forth are some run of the mill non-direct trademark loads utilized as a part of the greater part of the modern applications and are expanding quickly because of specialized changes of semiconductor gadgets, advanced controller and adaptability in controlling the power utilization. The utilization of the above power electronic gadgets in control dispersion framework offers ascend to sounds and receptive power aggravations. The music and responsive power cause various bothersome impacts like warming, hardware harm and electromagnetic impedance impacts in the power framework. In high power applications, the multilevel inverters are more sufficient contrasted with the traditional two-level structure. The numerous inalienable advantages of these structures have prompted their current expanded enthusiasm among both industry and utilities. The unbalance of the distinctive DC voltage wellsprings of the multi levels inverters constitutes the significant restriction for the utilization of these power converters. A few strategies are proposed to smother the unbalance of nonpartisan point potential. Some of these strategies depend on including a zero arrangement or a dc-balance to yield voltage [1,2]. In [3,4], control hardware is added to redistribute charges between capacitors. A technique in light of limiting a quadratic parameter that relies upon capacitor voltages is exhibited in [5]. This quadratic parameter is emphatically characterized and achieve zero when the two capacitors have a similar voltage.
Some different works utilize a converter-inverter course, and apply programmed control strategies, for example, fluffy rationale control [6] or sliding mode control [7] to this course. In this work we utilize a straightforward shut circle strategy which makes a nonstop estimation of yield current and contrast between capacitors voltages, and pick the repetitive vector based on these estimations.

In this paper, initial segment is devoted to the introduction of the model of the three stages five-level diode braced voltage source inverter (VSI) with its space vector graph. In the second part, the proposed disentangled SVPWM control technique is introduced [8]. After that the multi DC transport voltages adjusting technique utilizing excess vectors is nitty gritty. This APF is connected for the upgrade of medium voltage arrange control quality by pay of consonant streams created by a lopsided nonlinear load (Figure 1). Toward the end the reproduction aftereffects of sliding mode controlled APF are exhibited.

![Synoptic diagram of application of shunt APF on power supply fed a non-linear load](image)

Fig.1 Synoptic diagram of application of shunt APF on power supply fed a non-linear load
2 Modeling and control of five-level Diode Clamped VSI

2.1 Modeling of five-level Diode Clamped VSI

Structure of five-level diode clipped inverter is appeared in Figure 2. Every leg is made out of four upper and lower switches with against parallel diodes. Four arrangement dc-interface capacitors split the dc-transport voltage down the middle. The fundamental conditions for the exchanging states for the five-level inverter are that the dc-connect capacitors ought not be shorted, and the yield current ought to be constant [9].

![Fig.2 Five-level diode clamped voltage source inverter](image)

Each leg of the inverter has five possible switching states (Tab.1):

**State P2:** The upper switching devices S1x, S2x, S3x and S4x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage \( V_{xn} = E/2 \).

**State P1:** The switching devices S2x, S3x, S4x and S5x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage \( V_{xn} = E/4 \).

**State 0:** The switching devices S3x, S4x, S5x and S6x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage \( V_{xn} = E/4 \)
3) are turned on. The output phase to neutral point voltage \( V_{xn} = 0 \).

**State N1:** The switching devices \( S_{4x}, S_{5x}, S_{6x} \) and \( S_{7x} \) \((x = 1, 2 \text{ or } 3)\) are turned on. The output phase to neutral point voltage \( V_{xn} = -E/4 \).

**State N2:** The lower switching devices \( S_{5x}, S_{6x}, S_{7x} \) and \( S_{8x} \) \((x = 1, 2 \text{ or } 3)\) are turned on. The output phase to neutral point voltage \( V_{xn} = -E/2 \).

For each switching device \( S_{ij} \) \((i = 1-8, j = 1,2 \text{ or } 3)\), we define a Boolean function \( F_{ij} \) as:

**Table 1 States of five-level inverter**

<table>
<thead>
<tr>
<th>Switching Symbols</th>
<th>Switching States</th>
<th>Output Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_1 )</td>
<td>ON ON ON ON OFF OFF OFF OFF</td>
<td>( E_1 )</td>
</tr>
<tr>
<td>( P_1 )</td>
<td>OFF ON ON ON OFF OFF OFF OFF</td>
<td>( E_2 )</td>
</tr>
<tr>
<td>( O )</td>
<td>OFF OFF OFF ON ON OFF OFF OFF</td>
<td>( 0 )</td>
</tr>
<tr>
<td>( N_1 )</td>
<td>OFF OFF OFF ON ON OFF OFF OFF</td>
<td>( -E_4 )</td>
</tr>
<tr>
<td>( N_2 )</td>
<td>OFF OFF OFF ON ON OFF OFF OFF</td>
<td>( -E_2 )</td>
</tr>
</tbody>
</table>

Since five kinds of switching states exist in each leg, this converter has 125 switching states. The output voltage vector can take only 61 discrete positions in the diagram because some switches state are redundant and create the same space vector.
2.2 Simplified SVPWM for five-level inverter

The space vector graph of a five-level inverter can be suspected that is made out of six hexagons that are the space vector charts of the three-level inverters [10]. Every one of these six hexagons, constituting the space vector chart of a three level inverter, focuses on the six peaks of the medium hexagon as appeared in Figure 4.

Fig.4 Simplification of a 5-level SV diagram into 2-level SV diagram

To streamline into the space vector chart of a three-level inverter, two stages must be taken.
Right off the bat, from the area of a given reference voltage, one hexagon must be chosen among the six hexagons. There exist a few locales that are covered by two contiguous hexagons. These areas will be isolated in fairness between the two hexagons as appeared in Figure 5. Every hexagon is distinguished by a number S characterized in condition (5).

Furthermore, we interpret the beginning of the reference voltage vector towards the focal point of the chose hexagon as demonstrated in Figure 6. This interpretation is finished by subtracting the middle vector of chose hexagon from the first reference vector. Table 2 gives the parts d and q of the reference voltage $V_3^*$ after interpretation, for all the six hexagons. The list (5) or (3) over the parts show five or three-level cases separately.
Table 2 Correction of 5-level reference voltage vector

<table>
<thead>
<tr>
<th>s</th>
<th>$v_{i_1}^{5s-1/2}$</th>
<th>$v_{i_2}^{5s-1/4}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$v_{i_1}^{5s-1/2}$</td>
<td>$v_{i_2}^{5s-1/4}$</td>
</tr>
<tr>
<td>2</td>
<td>$v_{i_1}^{5s-1/4}$</td>
<td>$v_{i_2}^{5s-3/4}$</td>
</tr>
<tr>
<td>3</td>
<td>$v_{i_1}^{5s+1/4}$</td>
<td>$v_{i_2}^{5s+3/4}$</td>
</tr>
<tr>
<td>4</td>
<td>$v_{i_1}^{5s+1/2}$</td>
<td>$v_{i_2}^{5s+3/2}$</td>
</tr>
<tr>
<td>5</td>
<td>$v_{i_1}^{5s+1/4}$</td>
<td>$v_{i_2}^{5s+3/4}$</td>
</tr>
<tr>
<td>6</td>
<td>$v_{i_1}^{5s-1/4}$</td>
<td>$v_{i_2}^{5s+3/4}$</td>
</tr>
</tbody>
</table>

At the end, one applied the pulse width modulation based on voltage space vectors of H. W. Van Der Broeck [11]:

Fig.6 Translation of 3-level reference voltage vector

Table 3 Correction of 3-level reference voltage vector

<table>
<thead>
<tr>
<th>s</th>
<th>$v_{i_1}^{3s-1/4}$</th>
<th>$v_{i_2}^{3s-1/4}$</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>$v_{i_1}^{3s-1/4}$</td>
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<td>$v_{i_1}^{3s-1/4}$</td>
<td>$v_{i_2}^{3s-3/8}$</td>
</tr>
<tr>
<td>3</td>
<td>$v_{i_1}^{3s+1/4}$</td>
<td>$v_{i_2}^{3s-3/8}$</td>
</tr>
<tr>
<td>4</td>
<td>$v_{i_1}^{3s+1/4}$</td>
<td>$v_{i_2}^{3s+1/8}$</td>
</tr>
<tr>
<td>5</td>
<td>$v_{i_1}^{3s+1/4}$</td>
<td>$v_{i_2}^{3s+3/8}$</td>
</tr>
<tr>
<td>6</td>
<td>$v_{i_1}^{3s-1/4}$</td>
<td>$v_{i_2}^{3s+3/8}$</td>
</tr>
</tbody>
</table>
3 Redundant vectors algorithm for 5-level APF

In this section, one proposes to solution for the unsteadiness issue of the info DC voltages of five-level APF, by utilizing the repetitive vectors of this topology. To know the effect of every vector on capacitors voltages, four stages must be taken after:

Initial one comprises in meaning of conditions speaking to capacitors streams as an element of load ebbs and flows for every vector with excess states. Tables 4,5,6 resume connections between stack streams and capacitor ebbs and flows for all the repetitive vectors of the space vector outline.

To diminish the extent of control calculation, the second step comprises in constituting vectors bunches that have a similar aura in the table of states D1, D2 and D3. Table 7 demonstrates six conceivable instances of demeanor of states D1, D2 and D3. The distinctive gatherings are recorded roar:

Group 1: V1, V4, V7, V10, V13, V16
Group 2: V2, V6, V8, V12, V14, V18
Group 3: V3, V5, V9, V11, V15, V17
Group 4: V19, V21, V23, V25, V27, V29
Group 5: V20, V22, V24, V26, V28, V30
Group 6: V31, V32, V33, V34, V35, V36

Third step comprises in investigating the impact of various gatherings of repetitive vectors on capacitors voltages, under various states of load streams. From Table 7, it can be seen that a few vectors rely upon state D1 (bunches 1, 4 and 6) and others rely upon states D1, D2 and D3 (bunches 2, 3 and 5).

For vectors relying upon state D1, there are two conceivable outcomes of extremity as indicated by stack streams. Every probability is related to rationale work in the accompanying way:

4 Sliding mode control of APF

Dynamic power channel is controlled utilizing sliding mode controller [12,13]. From the model of dynamic channel related to sup-

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ply arrange (8) and by considering the mistake between symphonic current reference and the dynamic channel present as sliding surface (9), and the smooth nonstop capacity as alluring control work (10), one gains the power law (11).

\[
V_{\text{ref }, K} - V_{\text{K}} =
\]

\[
I_{\text{V}_{\text{K}}} = V_{\text{sk}} - \dot{R}_{\text{sk}} \ast i_{\text{sk}} - L_{\text{sk}} \ast (f_{\text{c}})
\]

\[
V_{\text{fref }, k} = \dot{R}_{\text{f}} \ast i_{\text{f}} + L_{\text{f}} \ast (f_{\text{c}}) + \{ f_{\text{d}} \} \ast \{ f_{\text{ref}, k} \}
\]

5 Simulation Results

A medium voltage wellspring of 5.0kV, 50Hz bolsters a non-direct load as outlined in Figure 1. This heap produces mutilated stages streams with add up to symphonious contortion (THD) of separately 120%, 129% and 83% which is over the endured THD constrain standard. These streams with there ghostly investigation are displayed in Figure 8.

The initial segment of this reenactment is committed to researching the execution of the Redundant Vectors Control Algorithm (RVCA). For that, dynamic power separating is presented at \( t=2s \) without connected RVCA. One comments that capacitors voltages separate (Figure 9). Utilization of the proposed RVCA based SVPWM at \( t=5s \), drive capacitors voltages towards the reference estimation of 3 kV keeping them consistent. The second part is devoted to testing the performance of the APF. As shown in Figure 9, at \( t=7s \), the resistor value changes from \( R_2 = 300 \Omega \) to \( R_2 = 100\Omega \). This resistor variation implies the increase of the non-linear load current amplitude. The capacitors voltages are not disturbed by this load variation (Figure 8).

Figure. 7. a, b, c presents main source voltages and currents after harmonic currents compensation. Spectral analysis of each current is illustrated in Figure. 9 d,e,f. It is shown that source currents are almost sinusoidal with THD low than 3%.

Simulation Parameters:
Main source:
\( V_{\text{ph-ph}} = 5.0k \text{V, } f = 50 \text{ Hz, } R_s = 0.0005\Omega. \)
$L_s = 0.005 \text{H.}$

Load:-
$C_1 = C_2 = 0.1 \text{ F, } R_1 = 200, R_2 = 300 \Omega$ (t = 2s),
$R_2 = 100 \Omega$ (t = 7s).

Active power filter:-
$R_f = 0.0005 \Omega, L_f = 0.004 \text{ H, } C = 0.01 \text{F, } f_c = 2 \text{kHz.}$

Fig.7 Current drawn by the non-linear load

Fig.8 DC bus capacitors voltages of five-level APF
6 CONCLUSION

This paper exhibits a calculation for self adjustment of dc interface capacitors voltages utilizing excess vectors of five-level diode clasped shunt dynamic power channel. An exhaustive investigation of the dc interface capacitor voltages adjusting is exhibited. In view of the estimation of load streams and assurance of capacitor ebbs and flows signs, the attractive repetitive vector is chosen. Likewise, a disentangled space vector beat width regulation calculation has been portrayed and connected to five-level inverter. Through the decay of the space vector outline the entangled five-level space vector balance calculation is improved into two-level cases. This streamlined SVPWM technique has the focal points to lessen the execution time of the five-level inverter regulation and permits sparing memory of the controller in the event of trial acknowledgment. With a low exchanging recurrence the proposed repetitive vectors control makes conceivable:

- Stable multi DC interface voltages without utilizing extra power gadgets hardware;
- Active power sifting in medium voltage without utilizing transformer.
• Low add up to consonant mutilation of fundamental source streams.
• Compensation of responsive power.

References


