ANALYSIS OF CLOCKFEEDTHROUGH ERROR REDUCTION IN CMOS ANALOG AND DIGITAL CIRCUITS AT 180 nm TECHNOLOGY NODE

Udari Gnaneshwara chary, J. Yeshwanth Reddy, L. Babitha, I. Balarama Krishnam Raju.
1,2,3 Asst. Professor, 4Assoc. Professor,
Department of ECE,
BVRIT, Narsapur, Medak.

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Abstract

An analysis of different reduction techniques for clock feed-through (CFT) error in Switch capacitor CMOS analog circuits is presented. In this paper, the working mechanism of four different reduction techniques and its pros and cons are described, and a comparison of CFT error in different circuits implementation in cadence virtuoso 180nm CMOS Technology is also Discussed. The simulation results have verified that the proposed techniques are insensitive to the non-ideal effects. In addition to these its effectiveness has also been validated by the experimental results.

Keywords: Clock feed-through, charge injection, analog switch, switch capacitor circuits, integrated circuits.
1 INTRODUCTION

Switched capacitors are designed by using active resistors called MOSFETs. Which are mainly used in analog circuits such as active filter circuits, sampling and hold circuits. This circuits are suitable for interfacing analog to digital circuits and Digital signal processing circuits etc. Advances in CMOS technology, however, are driving the operating voltage of integrated circuits increasingly lower. As device dimensions shrink, the applied voltages will need to be proportionately scaled in order to guarantee long-term reliability and manage power density. The reliability constraints of the technology dictate that the analog circuitry operates at the same low voltage as the digital circuitry. An analog switch is a basic component in integrated circuits (ICs). The on/off behavior of an analog switch is controlled by the gate voltages that govern the presence of charge in the inversion channel underneath the gates. However, MOS analog switch is not an ideal switch. The injection of parasitic charges from the channel and gate-drain/gate-source overlap capacitances into source and drain terminals degrade the performance.

This is one of the major limiting factors in high precision and fast analog switching circuits. Because of its importance, an accurate analysis of this effect is critical in the simulation of switching circuits and development of error cancellation techniques. A low sensitivity with finite gain has been achieved in the switched-capacitor integrator which also has very less area when compared to uncompensated integrator [2]. High-Resolution pipelined analog to digital converters does accurate multiply-by-two(x2) function using capacitor error-averaging technique. Digital Calibration and trimming is not required for correcting the errors due to capacitor mismatch and switch feed through in the analog domain [3]. The evolution technology is not so supportive for the analog circuits so many processing functions to be converted into analog to digital domain which in turn has applications like reduction of power consumption and size of chip, improves the design Process [4].

The pipeline A/D Converter with low voltage and low power is used for the video rate applications [5]. A technique of Gate-Source bootstrap is further modified with the input of switched Op-Amp circuit [6]. Under Very low voltage switch operation con-
ditions, the switch conducts in both linear and saturation region. The switch sizing has allowed minimizing clock feed through for a very low voltage Delta sigma modulator which is implemented in automatic sizing tool [7]. The circuit with gate of transistor and bulk node tracks the input signal of the bootstrapped switch which is implemented in a standard CMOS Technology [8].

In Section II, a clear understanding of both CI error and the CFT error are illustrated. Section III proposes the different reduction techniques of Clock feed-through error in analog MOS switch. Then a comparison of clock feed-through error in different cmos circuits are presented in Section IV. After all, Experimental results and its performance comparisons are illustrated. Finally, the conclusions are drawn are presented in section V.

2 CLOCK FEEDTHROUGH AND CHARGE INJECTION EFFECT

This section illustrates the mechanism of basic switch operation and errors arise during the switch in OFF state. The operation of an analog switch is demonstrated by the simple sample and hold circuit as shown in fig1.

Figure 1: Sample and Hold Circuit
At high voltage $(VG = VH)$, (this is the sampling phase, more appropriately the tracking phase for this circuit), the transistor operates in the triode region, acting like a linear resistor between the voltage source and the sampling capacitor, letting charge flow on to the top plate of the capacitor. When the gate voltage is low (this is the holding phase), the transistor operates in cutoff and the electrical link between the capacitor and the voltage source is broken, thus, the capacitor retains whatever charge, and thus voltage, it had in the sampling phase. This is an ideal case of sample and hold circuit operation.

An MOS transistor cross sectional view shown in fig 2 holds mobile charges in its channel when it is on. When the Transistor turns off, some portion of the mobile charges is transferred to the hold capacitor and causes an error in the sampled voltage (see Fig. 3).

The turnoff of an MOS switch consists of two distinct phases. During the first phase[A to B], the transistor is on and a conduction channel extends from the source to the drain of the transistor. As the gate voltage falls, mobile charges exit through both the source end and the drain end. When the gate voltage reaches the threshold voltage, the conduction channel disappears (see Fig. 4).

The total charge expressed in the inversion layer when the transistor is ON is

\[ Q = \int_{S_i}^{d} \rho \, dA \]
Figure 3: MOS Switch Charge injection Problem

\[ Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{th}) \]  

Where \( L \) denotes the effective channel length. When the switch turns off, \( Q_{ch} \) exits through the source and drain terminals, a phenomenon called channel charge injection. The charge injected to the left side on Fig.4 is absorbed by the input source, creating no error. On the other hand, the charge injected to the right side is deposited on \( C_h \) introducing an error in the voltage stored on the capacitor. For example, if half of \( Q_{ch} \) is injected onto \( C_h \) the resulting error equals

\[ \Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{th})}{2C_h} \]  

Note that the error is directly proportional to \( WLC_{ox} \) and inversely proportional to \( C_h \). Now, the transistor enters into the second phase [B to C] of turnoff. During this phase, only the clock feed-through through the gate-drain overlap capacitance (\( C_{gd}, C_{gs} \)) continues to increase the error voltage (see Fig.5).

This effect introduces an error in the sampled output voltage. Assuming the overlap capacitance is constant, we express the error as

\[ \Delta V = V_{clk} \frac{W_{cov}}{W_{cov + C_h}} \]  

5
Therefore, charge injection, clock feed-through leads to a trade-off between speed and precision as well.
3 TECHNIQUES FOR REDUCTION OF CLOCK FEED-THROUGH ERROR

To reduce the clock feed-through error four different techniques have been implemented.

1. Use of Dummy Switch. 2. CMOS Sampling Switch. 3. Bootstrapping Switch. 4. Injection Nulling Switch.

Use of Dummy Switch: Interestingly, with the choice \( W2 = 0.5W1 \) and \( L2 = L1 \), the effect of clock feed-through is suppressed shown in fig 6.

Overlap Capacitor \( [C_{gd}] \) effect injected by main transistor M1 can be removed by means of second transistor. After M1 turnoff M2 turns ON, the channel charges deposited by the former on Ch is absorbed by later to create channel. This technique is effective.
only if exactly half of charges stored in M1 is transferred to M2.

To guarantee half of charge goes to each side create the same environment on both sides. Add capacitor equal to sampling capacitor to the other side of the switch add fixed resistor to emulate input resistance. But, this Dummy switch technique Degrades sampling bandwidth.

Transmission Gate Switch: Fig 7 shows Another approach to lowering the effect of clock feed-through incorporates both PMOS and NMOS devices [10] such that the opposite overlap capacitances injected by the two cancel each other. Transmission gates were used extensively in the switched-capacitor gain stages of the pipeline, because it eliminates the undesirable threshold voltage effects which give rise to loss of logic levels in single pass transistor.

![Figure 7: TG switch with sample and hold Capacitor](image)

\[
\frac{V_{G_{PMOS}}}{V_{G_{PMOS}+Ch}} = \frac{V_{G_{NMOS}}}{V_{G_{NMOS}+Ch}}
\]  

(4)

The advantage of this technique is Clock feed-through problem diminished and the ON resistance thus propagation delay would be half the value of single NMOS transistor, but use of complementary gates require more area. Fig 8 shows the transient analysis of TG switch.

Bootstrap switch: A critical problem in designing analog sampled-data systems (like SC circuits, ADC) operating at low-
voltage supply is the MOS switch. Using a NMOS switch as a sampling switch in the T/H circuit has main issue of input-dependent finite ON-resistance given by:

\[ R_{on} = \frac{1}{\frac{\mu}{2}(V_{gs}-V_{th})} \]  

(5)

Since \( V_{gs} = V_{dd} - V_{in} \)

Here \( R_{on} \) is signal dependent and results to be more resistive (performing lower bandwidth) at low supply voltage. This problem is more critical when \( V_{DD} \) decreases as in scaled technologies. A popular solution is the use of a bootstrapped switch. The bootstrapped MOS switch achieves rail-to-rail signal swing at low voltage without requiring low-threshold devices. It overcomes the threshold voltage drops of the output voltage levels.

In off state, the gate is grounded and the device is cutoff. In the on state a constant voltage of \( V_{DD} \) is applied across the gate to source terminals. A Low and constant on-resistance is established from drain to source independent of the input signal.

An improved actual bootstrapped circuit applied on a MOS switch as shown in fig.9 and fig 10 shows the transient analysis of bootstrapped switch.

During on-state the gate-to-channel voltage is kept constant, guaranteeing constant switch conductance. This is done by connecting a capacitance (precharged at \( V_{DD} \) during the off-state) be-
Figure 9: Bootstrap Switch Circuit

Figure 10: Transient analysis of Bootstrap Switch
tween the gate and source terminals of the main Switch. VDD is applied across capacitor C3 by M3 and M12. This capacitor will act as the battery across the gate and source during the on phase. When goes high, allows charge from the battery of capacitor C3 to flow onto the gate G. This turns on both M9 and M11. M9 enables the gate G to track the input voltage S shifted by VDD, keeping
the gate-source voltage constant regardless of the input signal. This effect introduces an error in the sampled output voltage. Assuming the overlap capacitance is constant, we express the error as

![Figure 11: General structure of INS to CFT error](image)

<table>
<thead>
<tr>
<th>Reduction Method</th>
<th>Error Voltage</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch</td>
<td>4.90mV</td>
<td>1.77nW</td>
</tr>
<tr>
<td>Dummy Switch</td>
<td>3.98mV</td>
<td>4.85nW</td>
</tr>
<tr>
<td>Transmission gate switch</td>
<td>0.78mV</td>
<td>0.48nW</td>
</tr>
<tr>
<td>Bootstrapping Switch</td>
<td>0.09mV</td>
<td>0.33nW</td>
</tr>
</tbody>
</table>

Table 1. Error voltage results of 4 S/H circuits

4 CONCLUSION

Clock feed through errors are analyzed for MOS switch, transmission gates and Bootstrapping switch circuits. By applying error reduction techniques errors are reduced which are shown in transient analysis and experiment is done on cadence virtuoso 180 nm technology.
References


