AN EFFECTIVE LOW POWER HIGH GAIN OP-AMP DESIGN FOR BIO-MEDICAL APPLICATION

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Abstract

operational amplifier (Op-Amp) topology that achieves high-gain and low-power dissipation is designed and analyzed. The low power operational amplifier is the main active power consuming. The Operational Amplifier (Op-Amp) is a fundamental building block in Mixed-Signal design. Two stages Op-Amp is one of the most commonly used Op-Amp architectures. Most CMOS Op-Amps are designed for specific on-chip applications. The result shows the Op-Amp consumes a total power of 1.80mW with the gain 95dB. This design has been implemented using the 32 nm CMOS technology.

Keywords: Bio-medical, Operational Amplifier, CMOS Technology
1 INTRODUCTION

An operational amplifier is the basic building blocks of analog electronic circuits. They are linear devices with all properties of a dc amplifier. Op Amp is many Different Ways to make them Different Forms Of amplifier available such as Inverting amplifier, Non-Inverting amplifier, Voltage Follower, Comparator and Differential amplifier, Integrator Etc. Op amp have the excellent performance with very low input current and voltage. The increasing demand for portable equipment and its applicability in bio-medical applications has enhanced the importance of low power circuit design. Circuit designs with low power dissipation are reported recently, significant efforts have been invested in reducing power consumption of the operational amplifiers and developing circuits that operate with extremely small voltage supply, however it is envisaged that the implementation of the low-power circuit design is limited by many factors.

The most dominating factors in determining the performance of low-power system design are the gain of the system. For achieving high-gain in a system, the high supply voltage is needed. Another important constraint that limits the use of small supply voltage is signal-to-noise ratio (SNR). In CMOS circuits, the dynamic power consumption is quadratically dependent to the supply voltage. The reduction in power consumption as the supply voltage decreases. But in analog CMOS circuits sharing the same supply voltage, results in an increase in power dissipation in order to achieve the same SNR. Low-power and high-gain are particularly the major requirements monitoring and recording bio-potential signals (heart, brain, pulse etc.) for medical diagnosis. Modern clinical practice requires these signals to be routinely recorded. It is usually the practice that patients are connected to cumbersome recording devices for the purpose of acquiring signals from the body to aid diagnosis. This affects their mobility and causes general discomfort. This affects the general diagnosis of ailments.

The coupling of bio-potential signals from the body into the electronic equipment is accomplished through electrodes. These electrodes interface ionic currents in the body with electrical currents in the electronic instruments. In practice, because the
electrode comprises the first stage of the signal chain, its properties can dominate the overall noise and performance of the acquisition system making its design and selection crucially important.

Rapid developments in medical science have led to the daily use of biomedical equipment. The functions of biomedical equipment have become increasingly complex, along with the inbuilt electronic circuitry. The parameters under considerations are the gain, unity gain bandwidth (with capacitive load), slew-rate, phase margin and power consumption.

Operational amplifiers, the most commonly used building blocks in analog circuits, are usually considered as the design bottleneck in low-voltage and low-power applications, partially the analog to digital converters. In analog circuits, settling behavior of the Op-Amp usually determines the accuracy and speed of the circuit. High accuracy and fast settling require a high DC gain and a high unity-gain frequency, respectively. Thus a high-gain high-speed architecture in low-voltage applications is of much interest in the state-of-the-art amplifier designs.

The classical input differential stages (DS) of the operational amplifiers. Besides, their output current is restricted at the low levels of the input voltage. This effect is provided due to the application of the transistors with various principles of operation (bipolar, CMOS and JFETs). Low-power dissipation, high-input common mode range (ICMR), high-gain and high-phase margin are achieved.

It includes design of a low-power, high-gain and highly stable amplifier for biomedical applications. Low-power dissipation, high-input common mode range (ICMR), high-gain and high-phase margin are achieved. An operational amplifier can still be used for low speed - low switching applications such as sensor networks, and biomedical devices, where speed performances are not critical.

2 EXISTING SYSTEM

The Low-power and high-gain are particularly the using monitoring and recording bio-potential signals (heart, brain, pulse etc.) for
medical diagnosis is The low power operational amplifier is the main active power consuming block. The Op-Amp operates and supply voltage and consumes a total power. The Op-Amp operates at a $p_m 0.75V$ supply voltage and consumes a total power of 1.83mW with the gain 90dB. The design has been implemented using spice Tools for 90nm CMOS technology node.

3 PROPOSED SYSTEM

Operational Amplifiers are the backbone for many analog circuit designs. The speed and accuracy of these circuits depend on the bandwidth and DC gain of the Op-amp.

![Figure 1: Block diagram two-stage CMOS Op Amp](image)

Larger will be the bandwidth and gain, higher will the speed and accuracy of the amplifier. The general block diagram of an op-amp with an output buffer is shown above in Figure(1)

The simplified Block Diagram is shown in figure(2). The first block is a differential amplifier. It has two inputs, that are the inverting and non-inverting voltage. It gives a differential voltage at the output or a differential current which depends only on the differential input voltage.
The next block is a differential ended to the single-ended converter. It is used to transform the differential signal generated by the first block into a single-ended output signal. Some architecture does not require the differential to single-ended function; therefore this block can be eliminated in that.

In circuits where, the gain provided by the input stages is not sufficient, so there is an additional amplification is required which is provided by the second stage, the common source amplifier, driven by the first stage output. As this stage uses differential input unbalanced output differential amplifier, so it provides the required extra gain.

The biasing circuit is here to provide the proper operating point to each transistor in its saturation region. The output buffer stage provides the low impedance at the output and larger output current needed to drive the load of an op-amp or improves the slew rate.

Even the output stage can be dropped since many applications do not need low output impedance. If the op-amp is intended to drive a small purely capacitive load then output buffer is not required. When the output stage is not used the circuit is an operational transconductance amplifier, OTA. The motive of the compensation circuit is to decrease the gain at high frequencies and to maintain stability when negative feedback is applied to the op amp.

Designing of two-stage op-amps is a multidimensional-optimization problem where optimization of one or more parameters may easily result into the degradation of others. Also, the gain bandwidth product which is constant puts challenges to the designers in designing the circuits for high DC gain and high bandwidth applications. Here the gain has been
increased by employing thin and long transistors into the design at output stage and wide transistors in the input stage. These techniques are able to increase the gain up to a great extent by increasing the output resistance and input trans-conductance respectively. Here the improvement in unity gain bandwidth has been done by increasing the bias current which decreases the DC gain and increases power dissipation little bit, still provides a good alternative control to increase bandwidth. Introduction of each stage in multi-stage op-amps exhibits an additional pole into the system which can create problems in stability.

Figure 3: Schematic Diagram of Op-Amp

As the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers in CMOS technology becomes more critical. A new method for determining the component values and transistor dimensions for CMOS Op-amps. The performance of an op-amp is characterized by a number of performance measures such as open-loop voltage gain, quiescent power, input-referred noise, output voltage swing, unity-gain bandwidth, input set voltage, CMRR, slew rate, an area so on.

These performance measures are determined by the design parameters, e.g., transistor dimensions, bias currents, and other component values. The CMOS amplifier design problem we consider in this paper is to determine values of the design parameters that optimize an objective measure while satisfying
speciations or constraints on the other performance measures. This design problem can be approached in several ways, for example by hand or a variety of computer-aided design methods, e.g., classical optimization methods, knowledge-based methods, or simulated annealing.

![Figure 4: simulation Output Waveform for op-amp](image)

The Op-Amp Output Achieves The Power Dissipation 1.80mw And Gain 95db, Gain Bandwidth 135MHZ. A new method that has a number of important advantages over current methods. We formulate the CMOS op-amp design problem as a very special type of optimization problem called a geometric program.

The most important feature of geometric programs is that the globally optimal solution can be computed with great efficiency, even for problems with hundreds of variables and thousands of constraints, using recently developed interior-point algorithms. Thus, even challenging amplifier design problems with many variables and constraints can be solved.

The fact that geometric programs (and hence, CMOS op-amp design problems cast as geometric programs) can be globally solved has a number of important practical consequences.

The sets of infeasible speciations are unambiguously recognized: the algorithms either produce a feasible point or a proof that the set of speciations. In particular, our method computes the absolute limit of performance for a given amplifier and technology parameters. For example, the method can be used
to simultaneously optimize the design of a large number of op-amps in a single large mixed-mode integrated circuit.

4 RESULT ANALYSIS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Exact design</th>
<th>Proposed design</th>
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<tbody>
<tr>
<td>Technology</td>
<td>90nm</td>
<td>32nm</td>
</tr>
<tr>
<td>Gain</td>
<td>93dB</td>
<td>95dB</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1.83mW</td>
<td>1.80 mW</td>
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<tr>
<td>Gain Bandwidth (GB)</td>
<td>130MHz</td>
<td>135MHz</td>
</tr>
</tbody>
</table>

5 APPLICATION

Operational Amplifier (Op-Amp) is the important basic of any analog circuit. The conventional operational amplifier has a high voltage gain differential input stage with a second stage having high voltage gain with the last stage called buffer stage. The first two stages are responsible for providing the overall voltage gain of the operational amplifier circuit. CMOS (Complementary metaloxidesemiconductor) circuit is a basic building block for designing operational amplifier because CMOS circuits have various advantages over BJT (Bipolar Junction Transistor) including power consumption and noise reduction. Our main aim is to keep biomedical applications in mind while designing the Op-Amp. In such applications, the amplifier (along with other necessary circuits) comes in direct contact with the human body.
6 CONCLUSION

The two-stage CMOS op-amp mainly achieves the power dissipation compared to the 90 nm CMOS technology, and the operates the supply voltage is reduced and the gain increases the 93db. High gain enables this circuit to operate efficiently in a closed loop feedback system, whereas high bandwidth makes it suitable for high speed applications. The designing of op-amps puts new challenges in low power applications with reduced channel length devices. Advancements which have appeared recently through new techniques and technologies, give us multiple alternatives in implementations. The 32nm CMOS technology overcomes 90nm CMOS technology as it reduces the power dissipation and the supply voltage. The proposed design two stage op-amp design can be used in bio-medical application.

References


