



DESIGN OF HIGH SPEED AND ENERGY EFFICIENT VOLTAGE LEVEL SHIFTER

R.Indumathi¹, Mr.M.Udhayavani²,
¹PG Student,
²Assistant Professor
Dept of ECE,
Vivekanandha College Of Engineering
For Women,
Tiruchengode, Tamilnadu, India,
r.indumathi14@gmail.com
udhram@gmail.com

July 4, 2018

Abstract

The paper presents a high speed and power-efficient voltage level- shifting circuit. It is capable of converting extremely low levels of input voltages into high output voltage levels. In the proposed circuit the efficiency of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit. Post layout simulation results of the proposed circuit in a 0.18- μ m technology demonstrate a total energy per transition of 157 fJ, a static power dissipation of 0.3 nW, and a propagation delay of 30 ns for input frequency of 1 MHz, low supply voltage level of $V_{DDL} = 0.4$ V, and high supply voltage level of $V_{DDH} = 1.8$ V.

Keywords: Level converter, low power, subthreshold operation, voltage level shifter.

1 INTRODUCTION

One of the most effective ways to reduce dynamic and short-circuit power consumption of digital circuits is lowering the value of the power supply voltage [1][3]. On the other hand, reducing the supply voltage increases the propagation delay of the circuits. In digital circuits where different parts are operating at different speeds, in which a low voltage (i.e., VDDL) is applied to the noncritical paths and a high supply voltage (i.e., VDDH) is applied to the analog and the high-speed digital blocks [2], [3]. In this system, level-shifting circuits are needed to convert the lower logic levels into the higher ones to provide correct voltage levels for the next digital blocks. In order to alleviate the degradation of the overall performance of the circuit, the required level shifters must be designed with minimum propagation delay, power consumption, and silicon area. In addition, the employed level shifters are used to have more power saving in the low-supply blocks. Hence, in this brief, a fast and power-efficient voltage level shifter is proposed, which is able to convert extremely low values of the input voltages. The rest of this brief is organized as follows. In Section II, some of the recently reported high-performance voltage level shifters are reviewed. The proposed circuit is introduced in Section III. Section IV presents the simulation results of the designed circuit verifying the efficiency of the proposed structure. Finally, this brief is concluded in Section V.

2 VOLTAGE LEVEL SHIFTER

One of the conventional level-shifting architectures is shown in Fig. 1(a). The operation of this circuit is as follows. When the input signal IN is “High = VDDL,” MN1 and MN2 are ON and OFF, respectively.

Therefore, MN1 tries to pull the node Q1 down. Consequently, MP2 is gradually turned on to pull the node Q2 up to VDDH and to turn MP1 off. Similarly, when the input signal is changed to “Low

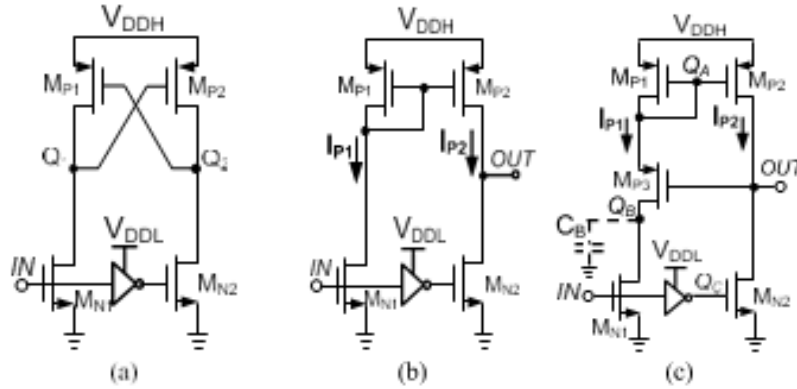


Figure 1: Schematic of the (a) conventional level shifter, (b) level shifter with a semi-static current mirror, and (c) level shifter with a dynamic current mirror (Wilson current mirror).

" = VSS," the operation is forced to reverse states. It is noticeable that, in this structure, there is a contention at the nodes Q1 and Q2 between the pull-up devices (i.e., MP1 and MP2) driven with VDDH and the pull-down devices (i.e., MN1 and MN2) driven with VDDL. As a result, when the voltage difference between VDDL and VDDH is high and particularly when the input voltage is in sub-threshold range, this circuit will no longer be able to convert the voltage levels. This is because the currents of the pull-down transistors are smaller than those of the pull-up devices.

To solve this problem, several attempts have been reported. One approach is to exploit technology-based strategies, e.g., employing strong pull-down devices using low-Vth transistors and/or weak pull-up networks by using high-Vth transistors [4]. Another approach is to use strong pull-down devices by enlarging their width, leading to an increase in both the delay and the power consumption. The last solution is to reduce the strength of the pull-up device when the pull-down device is pulling down the output node [5][9]. The structure illustrated in Fig. 1(b) uses a semi-static current mirror to limit the current and therefore the strength of the pull-up device (i.e., MP2) when the pull-down device is pulling down the output node. However, this structure suffers from the static current flowing through MN1 and MP1

during the “High” logic levels of the input signal [5][9]. In order to decrease the static power consumption, a dynamic current generator, which turns on only during the transition times, can be used. The structure is shown in Fig. 1(c) employs a dynamic current generator implemented by MP3 [5]. In this circuit, when the input signal IN goes from “Low” to “High,” MN2 turns off and MN1 turns on and pulls the node QB down. Since the node OUT had been “Low”(before the transition), during the time interval in which OUT is not corresponding to the logic level of the input signal IN, MP3 will be turned on. Therefore, a transition current flows through MN1, MP3, and MP1. This current is mirrored to MP2 (i.e., IP2) leading to pulling the node OUT up. Finally, when OUT is pulled up to VDDH, MP3 is turned off and therefore no static current flows through MN1, MP3, and MP1. On the other hand, when the input signal IN is changed from “High” to “Low,” MN1 turns off and MN2 turns on trying to pull the node OUT down

3 PROPOSED VOLTAGE LEVEL SHIFTER

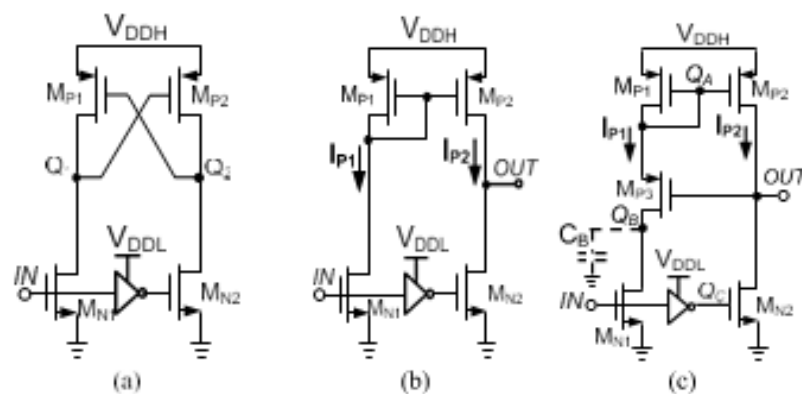


Figure 2: (a) Schematic diagram of voltage level shifter (b) Output waveform of voltage level shifter

In the proposed circuit, the transition current of IP2 must be

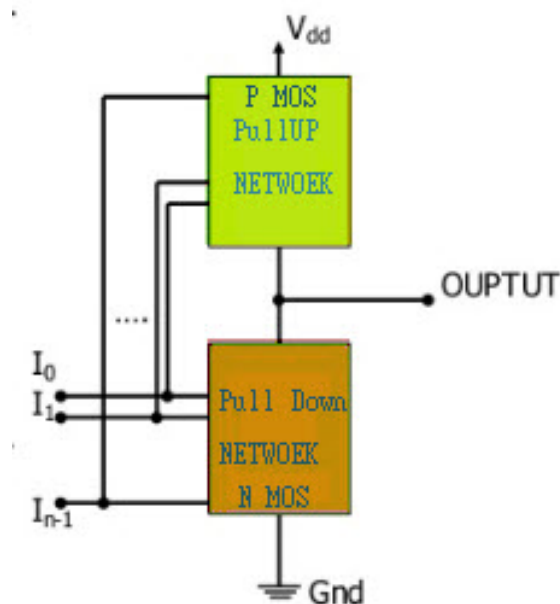
large enough to reduce the propagation delay of the low-to-high transition of the output voltage. On the other hand, the power consumption of the branch of MP1, MN1, and MN4 should be minimized. Therefore, the current mirror ratio (i.e., $(W/L) P2 / (W/L) P1$) should be large. For this purpose, the length of MP1 has been selected to be $5 \mu\text{m}$, whereas the lengths of the other devices are all chosen of minimum size (i.e., $0.18 \mu\text{m}$). Moreover, the width of MP2 is also selected to be $1 \mu\text{m}$. In addition, since MN2 is driven by a voltage lower than V_{DDH} , it must be somewhat strong to be able to pull the output node down. Hence, the width of this transistor is chosen to be 1 m , while the widths of the other transistors are of minimum size (i.e., $0.4 \mu\text{m}$). It is worth noting that not only the auxiliary circuit but also all the other structures, especially the one reproduced

In order to have a fair comparison between the structures, a unit buffer and an inverter are added as the load circuit and input buffer, respectively, to all the structures and the calculated power dissipation, includes the power consumption of these buffers. The transistors' sizes used for the performance comparison are shown. The transistor' sizes of the proposed circuit are shown

4 CMOS TECHNOLOGY

CMOS (Complementary Metal-Oxide-Silicon) technology, as compared with mature CCD (Charge-Coupled Device) technology, has the advantages of higher circuit integration, lower power consumption, and potentially lower price. The advantages make this technology competent for the next-generation solid-state imaging applications. However, CMOS processes are originally developed for high-performance digital circuits. Fabricating high-quality embedded image sensors with CMOS technologies is not a straightforward task. This motivates the study of CMOS technologies for imaging applications presented in this thesis. The major content of this study can be partitioned into four parts: (a) A two-stage characterization methodology is developed for sensor optimization, including the characterization of large-area photodiodes and comparative analyses on small-dimension sensor arrays with various pixel structures, junction types of the sensors,

and other process-related conditions. (b) The mechanism of hot-carrier induced excess minority carriers occurred at the in-pixel transistors is identified and investigated. The influence of the excess carriers on performance is analyzed. Suggestions on the pixel design are provided. (c) Signal cross-talk between adjacent pixels is quantified and studied using a sensor array with a specially designed metal shield pattern, which exposes the center pixel and covers the others.



The influence of cross-talk on color performance is analyzed. Process and layout improvements on cross-talk are also proposed. (d) The trend of pixel size reduction is investigated from the perspective of the achievable optical lens resolution. Using the modulation transfer function (MTF) as an index, optical simulations are performed to examine the relation between the lens resolution and the lens complexity

Frequency	$V_{DDL,min}$ (V)	Power (μ W)	Delay (ns)
5 MHz	0.38	0.98	45
10 MHz	0.41	1.68	24.3
20 MHz	0.44	2.77	13.65
50 MHz	0.49	5.72	5.81
100 MHz	0.54	10.2	2.86
200 MHz	0.6	17.66	1.46
500 MHz	0.72	47	0.63
1 GHz	0.9	95	0.34

5 RESULTS AND ANALYSIS

Simulation results of the proposed circuit ($V_{DDH} = 1.8$ v)

In the proposed structure, the typical PVT corner involves typical nMOS and pMOS transistors, a high supply voltage of $V_{DDH} = 1.8$ V, and a temperature of 25 °C. Moreover, slow-nMOS, fastpMOS, $V_{DDH} = 1.8\% + 10\% = 1.98$ V, and a temperature of 0°C were chosen as the worst corner. This is due to the fact that a larger difference between V_{DDL} and V_{DDH} as well as fast-pMOS and slow-nMOS increasing the mentioned contention between the pull-up and the pull-down devices. In addition, in the subthreshold region, a lower temperature results in a smaller current for the devices leading to increasing the propagation delay. On the other hand, for the best corner, simulations show that the minimum delay occurred for fastnMOS, fast-pMOS, $V_{DDH} = 1.8\%10\% = 1.62$ V, and a temperature of 120 °C. Fig. 6 shows the simulation results of the delay and the power dissipation of the proposed level shifter versus the value of V_{DDL} , for the typical, worst, and best PVT corners. It can be observed that the circuit works correctly at all the PVT corners for an input frequency of 1 MHz. To study how the process and temperature variations as well as, the mismatch between the devices affect the operation of the proposed circuit, a 1000-point Monte-Carlo simulation has been performed. The normalized standard deviation values (σ/μ) of the delay and power dissipation are 0.56 and 0.32, respectively. In order to study the main contributor of the static current in the proposed circuit, consider the situation in which the input is "High." Since MN7 is OFF, the gates of MP6 and MP7 are pulled up until the value of

$V_{DDH} - V_{th}$. Therefore, a static subthreshold current (the main contributor of the static current) flows through MP7, MP5, and MN5. It should be noted that as V_{DDL} (the driven voltage of the gates of MP5 and MN5) increases, the drain-source voltage of MP7 is decreased leading to a smaller current in MP7 and therefore a smaller static current.

6 CONCLUSION

In this brief, a fast and low-power voltage level-shifting architecture was proposed which is able to convert extremely low-input voltages. The efficiency of the proposed circuit is due to the fact that not only the current of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased. Post layout simulation results verified the efficiency of the proposed circuit compared with other works, especially from the power consumption viewpoint.

In summary, the new inductor-based boosting technique shows promising results for improving V_{min} , access time, and power consumption. This novel resonant supply boosting concept was explored through theoretical modeling, simulation, and measured hardware. Although this paper provides only an initial investigation into resonant supply boosting, there are numerous avenues to further optimize the proposed technique, which may be beneficial for future low power processors, accelerators, and IoT applications.

References

- [1] Alioto. M, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 329, Jan. 2012.
- [2] Corsonello .P, Perri .S, and Frustaci.F, "Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology," in Proc. IEEE Int. Conf. Comput. Design (ICCD), Oct. 2015, pp. 499504.

- [3] Hosseini .S. R, Saber .M, and Lotfi .R, "A low-power subthreshold to above-threshold voltage level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 10, pp. 753757, Oct. 2014.
- [4] Lanuzza .M, Corsonello .P, and Perri .S, "Fast and wide range voltage conversion in multisupply voltage designs," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 2, pp. 388391, Feb. 2015.
- [5] Ltkemeier .S and Ruckert .U, "A subthreshold to above-threshold level shifter comprising a Wilson current mirror," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 9, pp. 721724, Sep. 2010.
- [6] Luo .S-C, Huang .C-J, and Chu Y.-H, "A wide-range level shifter using a modified Wilson current mirror hybrid buffer," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 6, pp. 16561665, May 2014.
- [7] Osaki .Y, Hirose .T, Kuroki .T, and Numa .M, "A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs," IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 17761783, Jul. 2012.
- [8] Usami. K. et al., "Automated low-power technique exploiting multiple supply voltages applied to a media processor," IEEE J. Solid-State Circuits, vol. 33, no. 3, pp. 463472, Mar. 1998.
- [9] Wang. A and Chandrakasan .A. P, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 310319, Jan. 2005.
- [10] Zhang. D, Bhide .A, and Alvandpour .A, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- μ m CMOS for medical implant devices," IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 15851593, Jul. 2012.
- [11] Zhang. Y, Zhang. F, Shakhsher. Y, Silver J.D, Klinefelter. A, Nagaraju. Boley M. J, Pandey. J, Shrivastava . A, Carlson E.J, Wood . A, Calhoun B.H , and Otis B.P , "A batteryless 19 W

MICS/ISM-band energy harvesting body sensor node SoC for ExG applications," IEEE J. Solid-State Circuits, vol. 48, no. 1, pp. 199213, Jan. 2013.

