DESIGN OF FINFET BASED ARRAY MULTIPLIER USING 14NM TECHNOLOGY

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Abstract
Multiplier plays a significant position in digital image processing and various other applications. Due to the requirement of electronic devices, there is an essential for low power and high-speed devices. In this paper three 4-2 compressors and 10 transistors (10T), a full adder is designed with 4-bit array multiplier. Array multiplier is well known due to its regular structure. Array multipliers are used since it reduces the addition count at each stage so that it can decrease the total power consumption in the design. The results show the reduction in power dissipation, power product delay, delay using the FinFET technology of 14nm. Hence the array multiplier is used in the application digital image processing.
1 INTRODUCTION

In applications such as VLSI, digital image processing and data mining which are capable to tolerate error, exact computing units are not necessary. They can be a substitute for their approximate multipliers. The Adders and multipliers form the key components in these applications. In approximate full adders are designed at transistor level and they make use of it in digital image processing applications [7]. Due to advance development, there is a requirement for low power, high speed and more packing density of integrated chips (ICs) so that the scaling of devices is predictable. However, the usage of CMOS technology reaches its limit due to the Short Channel Effects (SCE).

In array multiplier, the group of identical cells generates new partial product and accumulation of the product at the same time. To reduce hardware complexity of multipliers, truncation is broadly employed in fixed-width multiplier designs. Then a constant or variable correction term is included to balances quantization error that is introduced by the truncated part.

The approximation method of array multipliers deals with the accumulation of partial products, in terms of power consumption and delay.

To decrease the risk factor in the usage of a hardware device the array multipliers are designed in which the LSB bits of array multipliers are condensed during the formation of partial products. The proposed multiplier design eliminates an adder circuit in partial product accumulation. In the design of three 4-2 compressors, they use a partial product reduction tree which consists of 4-bit array multiplier. The major drawback of the existing compressor is that when it gives non-zero output for zero-valued inputs there is a major effect on the Mean Relative Error (MRE) [9]. The proposed design overcomes the existing problem in the circuit. This leads to better precision. The Logic complexity deals with a straight-forward application of approximate multiplier and compressors to the partial products. In this concise, the partial products are transformed to initiate

Keywords: Array Multiplier, Compressor, FinFET.
terms with different probabilities. The method is simple in array multipliers when compared to other approximate multipliers as the addition of partial products is done serially as well as in parallel.

The designed array multipliers replaced by the existing dadda multiplier and the comparison is done in terms of area, power, error, and achieves Highest Peak Signal Noise ratio (PSNR) values in image processing application. The array multiplier reduces the number of transistors which in turn reduces the delay and power dissipation. Double gate MOSFETs (DG-FET) is a MOSFET that has two gates to control the channel. The main advantage of DG-FET is that it improves SCE.

The technology of FinFET is interest because it has double gates that are self-aligned. The FinFET technology provides less static power consumption. The process in which the gate wraps around the Fin provides improved control over the channel, and that allows little current to leak through the body when the device is in the off state. This will lessen sub-threshold leakage and results in better performance when compared to CMOS technology.

2 PROPOSED MULTIPLIER

Array Multiplier:

The partial product matrix is formed in the first stage by AND gates. In this design, three compressor and full adders are used to reduce the partial product values. The proposed full adder is designed by using only 10T full adder and it is used in the final computation of the binary values. Power consumption is lower because array multiplier requires only less number of adders at each partial multiplication stages.

A. Algorithm for array multiplier

- The Multiplier circuit is based on add and shift algorithm. Each partial product is created by multiplying the one multiplier bit of the Multiplicand in the array multiplier.
- Then the multiplied values are shifted in terms of their bit orders and then added with the final resultant values.
addition can be performed with normal carry propagate adder in which array multiplier uses N-1 adders where N is known as multiplier length.

- This is obtained by using full adder and a half adder to reduce the number of rows in the matrix number of bits at each summation stage.

Hence a FinFET based conventional array is used to compute the final binary value by using the uncomplicated structure of array multiplier as shown in Fig.1.

**B. Approximation of Altered Partial Product**

The accumulation of generate and propagate signals is completed through column-wise. In the approximation of full-adder, one of the two XOR gates is altered with OR gate which produces sum and carry computation [9]. This results in the error in last two cases out of eight cases. The probability of
prediction is extremely low. As the amount of generate signals increases, the error probability increases linearly. However, the value of error also increases. In adders and compressors, XOR gates are likely to contribute to a high area and high delay. In addition to reducing other partial products, 3 approximate half-adders, 10 full-adders, and 3 approximate compressors are essential in the first stage to generate Sum' and Carry' signals.

\[ W = (X_1 + X_2) \quad \text{(1)} \]

\[ \text{Sum'} = W \oplus X_3 \quad \text{(2)} \]

\[ \text{Carry'} = W \cdot X_3 \quad \text{(3)} \]

**C. 4-2 Compressor**

The logic expressions for the outputs of the first design of the approximate 4-2 compressor is proposed in this design with 4 inputs and 2 outputs [7]. The proposed design is lower than in the exact design and also the total number of gates used in the proposed design is considerably less than an exact compressor.

![4-2 Compressor Diagram](image)

Figure 2: 4-2 compressor

The design of an approximate 4-2 compressor is further increased in performance as well as reducing the error rate. Thus
Table I shows the Truth Table of the proposed approximate 4-2 compressor. In this design, FinFET 14nm based three 4-2 compressor and 10T full adders are used to reduce the partial product at every stage. In this recent design, carry uses the right-hand side equation and Cout is always equal to Cin. Table I shows the Truth Table of the first proposed approximate 4-2 compressor.

\[
\text{Sum'} = ((X1 \times X2)' + (X3 \times X4)')
\]  

(4)

\[
\text{Carry'} = ((X1 \times X2)' + (X3 \times X4)')'
\]  

(5)

The 4-2 compressor consists of 10 transistors full adder which is mainly used to perform fast multiplication operations. It includes four inputs with sum’ and carry’ as the output as shown in Fig 3.

Figure 3: Block diagram of 4-2 compressor with full adders
2.1 PROPOSED ARRAY MULTIPLIER

The 4-bit array multiplier is designed with the new structure of 4-2 compressor and 10 transistors full adder. The Multiplier circuit is based on add and shift algorithm. The partial product of the array multipliers is transferred according to their bit values and then the resultant values are added. Thus addition operation can be performed with normal carry propagate adder.

The Proposed array multiplier shows reduced power consumption, delay, and Power Delay Product (PDP) when compared to existing designs. The proposed designs are simulated using the HSPICE simulation tool at 14nm FinFET technology.

<table>
<thead>
<tr>
<th>X4</th>
<th>X3</th>
<th>X2</th>
<th>X1</th>
<th>Carry'</th>
<th>Sum'</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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The array multiplier is designed and the inputs are given by the binary values and the final multiplication is done and the binary result is obtained as shown in Fig 4. Power consumption and delay are lower when compared to other multiplier design.
Consider the 4-bit array multiplicand with eight inputs A0, A1, A2, A3 and B0, B1, B2, B3 and the output is obtained between y0 to y7. The average delay is generated by this array multiplier is shown in Fig 5.

3 RESULT ANALYSIS

The 4-bit array multiplier is designed using FinFET technology. The design of array multipliers in terms of area, delay, power, Power Delay Product (PDP) are compared and shown in Table II.
Figure 5: Simulation output waveform of FinFET based array multiplier

Table 2: Comparison of array and dadda Multiplier

<table>
<thead>
<tr>
<th></th>
<th>Exact design</th>
<th>Proposed design</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS 65nm</td>
<td>Dadda Multiplier</td>
<td>FINFET 14nm</td>
</tr>
<tr>
<td>Array Multiplier</td>
<td>Power (mW)</td>
<td>Delay (ns)</td>
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<tr>
<td></td>
<td>2158.5</td>
<td>0.68</td>
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</table>
4 APPLICATION-IMAGE PROCESSING

To reduce Gaussian noise geometric mean filter is widely used in image processing applications. The geometric mean filter is better at preserving edge features than the arithmetic mean filter. For the wide purpose, two 16-bits per pixel gray-scale images with Gaussian noise are measured in which 3 × 3 mean filter is used [9], where every pixel of a noisy image is replaced with the geometric mean of 3 × 3 blocks of adjacent pixels centered about it.

The 8-bit multiplier is designed and the program is coded and simulated in Microsoft Visual Studio 2010 and the output image is shown in Fig 6. The Energy requires an exact and approximate multiplication process while performing geometric mean filtering of the images is established by using Synopsys Primetime. The impact on energy utilization and image quality is computed due to an exact dadda multiplier in which the voltage scaled from 1 to 0.85 V (VOS) [9]. The PSNRs and energy consumption are measured by using input image and a consequential output image of exact and proposed array multipliers.

5 CONCLUSION

An Approximation is applied using simple AND gate for the transformation of the partial products. Approximate half-adder, full-adder, and 4-2 compressor are planned to decrease remaining partial products. The 4-bit array multiplier is used with 10T full adders and the three compressor circuits that achieve a significant reduction in area and power consumption compared with exact designs. The 14nm FinFET technology overcomes CMOS technology as it reduces the short channel effect and current leakage. The proposed design of array multiplier design can be used in image processing applications with minimal loss in output quality while saving significant power and delay.
Figure 6: Image multiplication results (a) Multiplier 1, (b) Multiplier 2, (c) Multiplier 3, (d) Multiplier 4, (e) Multiplier 5, (f) Multiplier 6, (g) Multiplier 7, (h) Multiplier 8.
References


