



DESIGN OF 2D DWT ARCHITECTURE FOR IDENTIFICATION OF CAROTID ASYMPTOMATIC PLAQUE

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Abstract

In this paper, to design show VLSI architectures for lifting based 2D-Discrete wavelet transforms (DWTs) are proposed. In discrete wavelet transform architecture, it can use shift and add logic instead of a multiplier. This method logic used for area efficient and delay effects. The lifting logic is implemented with 45 nm technology. The results show that the proposed designs attain significant development compared with existing architectures.

Keywords: DWT

1 INTRODUCTION

This process Wavelets are corresponded to the effective time and frequency signal properties. DWT is mainly used for image coding

technique. DWT is used to decompose the input values into a set of low and high pass outputs. The low pass outputs are sending as input for next level of operation recursively. In multimedia applications, DWT is used to decrease the redundant information and hence the storage requirement of image pixels will be reduced. DWT is used in image processing for the analysis of multi-resolution. The image reconstruction, image fusion, and image coding can be done easily with DWT. The general architectures of DWT are lifting based. In this paper, we considered only the lifting based DWT architecture [1].

The lifting based DWT has an advantage over convolution based DWT. Here, the low pass and high pass filters are replaced by upper and lower triangular matrices. The DWT with decomposition levels 2 or 3, the image quality will be good and the degradation is reasonable. Beyond the decomposition levels of 2 or 3, the image quality will be reduced. Therefore, a number of decomposition levels in the implementation of our proposed Fig. 1 shows lifting based 3 levels DWT. Here, P and U represent predict and update modules. The input sample values are decomposed into odd and even sample values using the split unit. The output from update unit is sent to the next stage recursively. The 2D-lifting based discrete wavelet transform outputs can be produced in 2 steps, namely (1) row process and (2) column process. During the row process, each row of $N \times N$ -input signal matrix is 1D transformed and the results are stored in $N \times N/2$ buffer. After completing all the N rows of $N \times N$ -input signal matrix in row process, transpose matrix of the $N \times N/2$ -buffer is taken for column process. In column process, each row of transposed buffer matrix is 1D transformed and results are the final 2D-DWT values ($N/2 \times N/2$).

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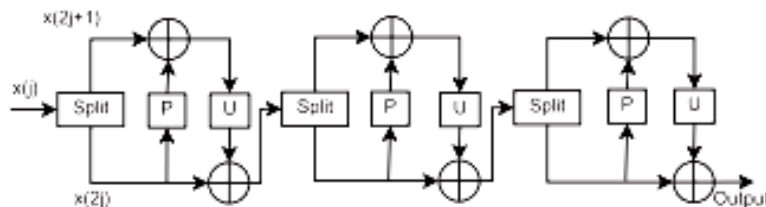


Figure 1: Lifting based DWT with 3 levels.

1.1 Lifting scheme

The DWT architecture of a lifting scheme that used for the correlation in the data to remove redundancy. First split the data into two sets (split phase) i.e., odd samples and even samples. Because of the unspecified softness of the data, we predict that the odd samples have a value that is closely related to their neighboring even samples. We use N even samples to predict the value of a neighboring odd value (predict phase). With a good calculation method, the chance is high that the inventive odd sample is in the same range as its prediction. We calculate the difference between the odd sample and its prediction and replace the odd sample with this difference. As long as the signal is highly interrelated, the newly designed odd samples will be on the normal smaller than the original one and can be represented with fewer bits. The odd half of the signal is now transformed. To transform the other half, we will have to apply the predicting step on the even half as well. Because the even half is merely a sub-sampled description of the original signal, it has lost some properties that we might want to protect. In case of images, we would like to keep the intensity (mean of the samples) constant throughout different levels. The third step (update phase) updates the even samples using the newly planned odd samples such that the desired property is conserved. Now the circle is round and we can move to the next level. We apply these three steps frequently on the even samples and convert each time half of the even samples, pending all samples are transformed.

2 EXISTING METHOD

Most of the 2D-DWT lifting based architectures use any one of the following 2D-DWT architectures (1) direct form; (2) recursive form; and (3) flipping form [7]. In all the above-mentioned architectures, the set of processing elements (PEs) are used. Each PE consists of two adders and one multiplier. The scaling constants (multipliers) are inverted to reduce the critical path delay of the lifting structure. In all these lifting based DWTs, the drawback is the worst path delay that includes two adders and one multiplier. In the proposed designs, it will use shift and add logic design instead of multipliers. Therefore, the worst path delay of proposed techniques is less than the existing designs. Another drawback with the above mentioned 2D-DWTs is the requirement of more cycles. In this paper, 2-parallel DWT architecture was implemented. In all the above-mentioned 2D-DWTs, the drawback is the requirement of more cycles and this has been resolved in our proposed N-parallel architectures. In the recent trends, multiple inputs and multiple output (parallel) lifting based architectures are proposed, where the transpose buffer is not used.

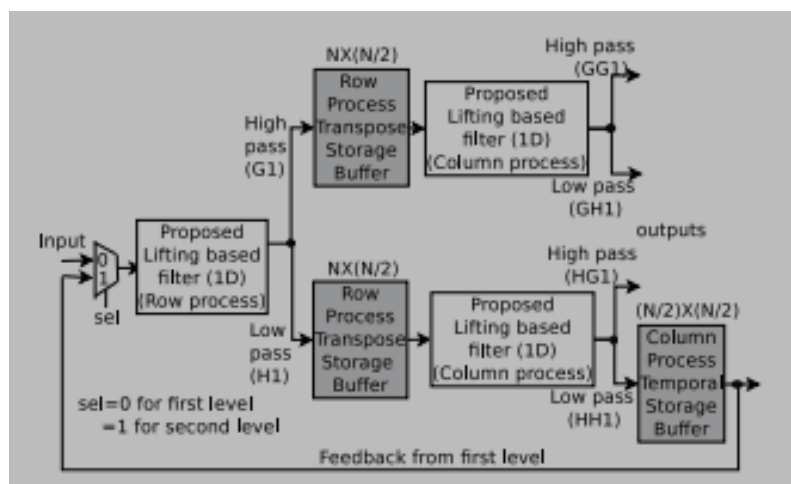


Figure 2: lifting based single PE N-point 2D-DWT architecture.

Therefore, the area for fast architectures is less than high-speed

design and the number of cycles for fast architectures is greater than high-speed design. Here, the drawback is the critical path that contains two add-shift based multipliers and four adders.

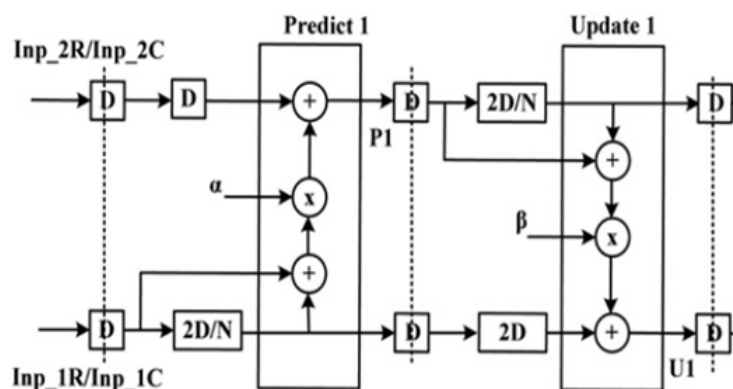


Figure 3: 2D DWT architecture with a multiplier

Therefore, the critical path of is much greater than proposed designs. The P-block parallel 2D-DWT is proposed in, where P 2 PEs are used in both row and column processes and each with four PEs. Therefore, require 4P multipliers and 8P adders in parallel to complete the DWT operation. In, M recursive architecture based PEs are used in row process and M direct form PEs are used in column process. In all the aforementioned transpose buffer free 2D-DWT parallel designs, the main drawback is the critical path delay that includes two adders and one multiplier, which has been reduced in the proposed designs.

3 PROPOSED METHOD

The major objective of this work is to optimize the delay, area and power requirement of lifting based 2D-DWT architecture. In general, any one of these parameters can be optimized at the cost of others. The proposed logic used for area efficient lifting based DWT is to perform the whole operation with one processing element. In this cases, it will use shift and add logic instead of multipliers. The

worst path delay for proposed techniques is less than other existing techniques because the existing techniques require two adders and one multiplier. In the proposed designs,

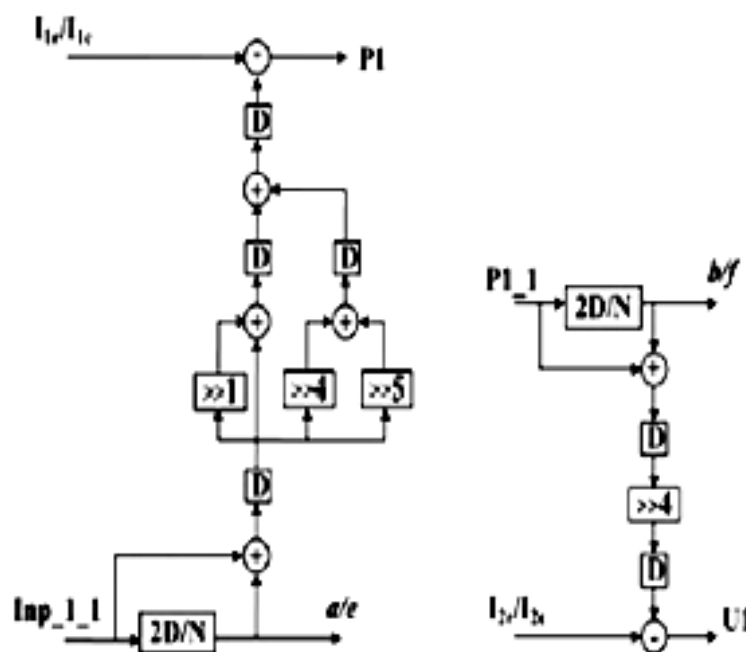


Figure 4: 2D DWT architecture using shift and add logic technique

there is no need to use multipliers. This circuit which will be used for area efficient and reduces the time delay.

A Detailed Data Flow Graph (DFG) of complete 9/7 lifting steps for the proposed two-input/two-output 1D row processing Element. Where each dashed line represents pipelining [2]. The predict module of the first lifting stage receives even and odd input at first clock cycle. The even input is added to earlier even input sample. Then multiplication with the first filter coefficient is performed in the second and third clock cycles by shift-and-add arithmetic. In the fourth clock cycle, multiplied result is added with the odd input sample to obtain first predict co-efficient. In

the fifth clock cycle, operation on present predict value and previous predict value along with previous even input give first update value. DFG shows that only adders are needed for the computation at each clock cycle, and thus the critical path is mainly limited to one adder delay only. Predict and update modules of first and second lifting stages are also fully pipelined to improve the operational speed. Predict and update modules of both lifting stages in RP and CP where the delay registrars 2D/N is used for row processor/column processors. The first lifting stage of the proposed architecture is designed using total seven adders/subtractors and four shifters. Similarly, the second lifting stage needs total ten adders and eight shifters.

4 DESIGN MODELING, IMPLEMENTATION, AND RESULTS

The existing 2D lifting based DWTs are modelled in Verilog HDL. These Verilog HDL models are simulated and synthesized using Quartus II software design tool with 45 nm technology that is used to find the worst path delay, area, power, and EOP details with operating voltage 0.88 v. which can be found by multiplying worst path delay with sum of dynamic (switching) and leakage (static) power.

4.1 Analysis of 2D-DWT architecture

The whole block of the 2D-DWT is implemented in Quartus II software the shift and adds logic based DWT was analyzed and synthesized

4.2 RTL view

Register-transfer level (RTL) of a digital circuit which will be used for design abstraction and also which will be used for models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers and the logical operations

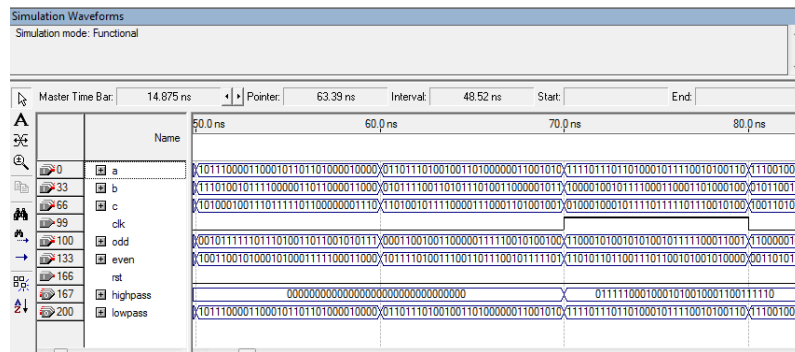


Figure 5: Simulation waveform of 2D DWT Architecture

performed on those signals. Design at the RTL level is typical practice in modern digital design.

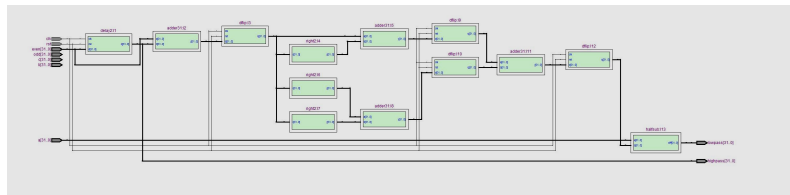


Figure 6: RTL view of 2D DWT Architecture without multiplier

4.3 logical elements

Logical element used in the circuit which will be reduced compared with the existing architecture.

Flow Status	Successful - Sat Dec 30 17:20:06 2017
Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	multiplierlessDWT
Top-level Entity Name	multiplierlessDWT
Family	Cyclone II
Met timing requirements	Yes
Total logic elements	235 / 14,448 (2 %)
Total combinational functions	201 / 14,448 (1 %)
Dedicated logic registers	167 / 14,448 (1 %)
Total registers	167
Total pins	226 / 315 (72 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)
Device	EP2C15AF484C6
Timing Models	Final

Figure 7: Logical element used in the DWT architecture

4.4 power and time analysis

The power and time analysis of 2D DWT Architecture without multiplier of a cyclone II Family which has to be analyzed.

Platform	Device	Logic Element		Power		Time	
		Existing	Proposed	Existing	Proposed	Existing	Proposed
Cyclone II	EP2C15AF484C6	6241	235	131.13	258.35	69.383	14.286
Cyclone III	EP3C10U484C6	6146	235	105.44	167.39	55.075	10.783
Stratix II	EP2S15F484C3	5987	168	361.09	500.69	45.398	7.688
Stratix III	EP3S10F484C2	5951	165	442.53	510.18	35.068	6.313

Table 1 Power and Time analysis of a 2D DWT architecture without multiplier

4.5 Logic element analysis of existing and proposed method

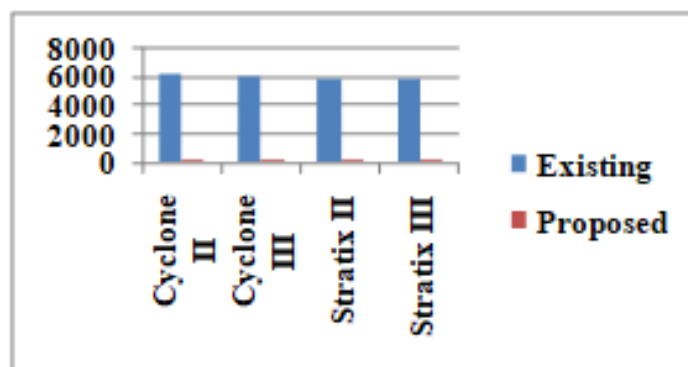


Figure 8: logic element analysis of existing and proposed

4.6 Power analysis of existing and proposed Method

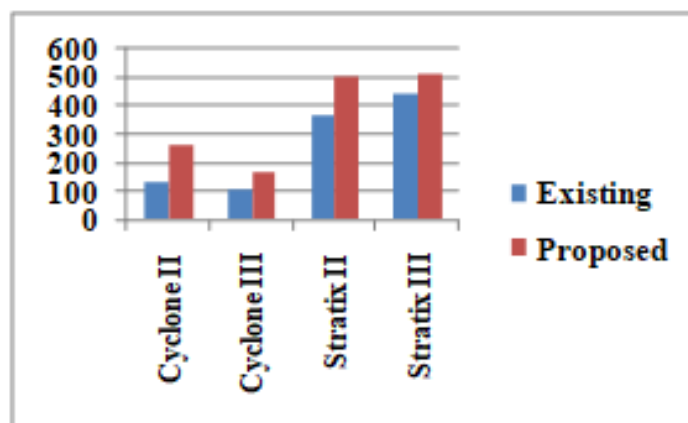


Figure 9: Powers analysis of existing and proposed

4.7 Time analysis of existing and proposed method

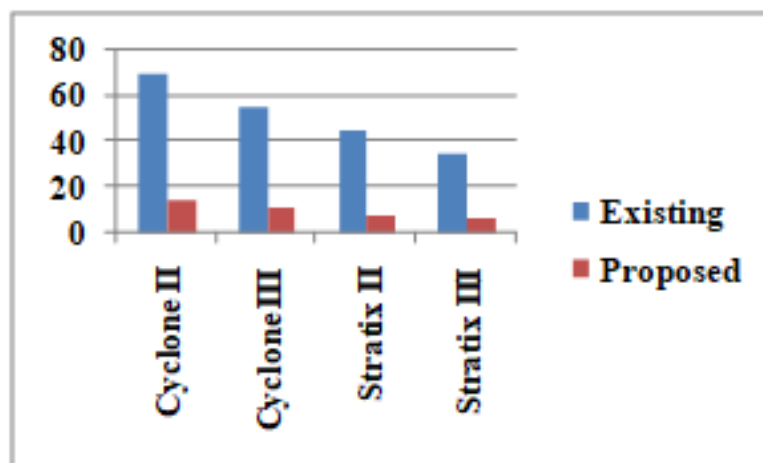


Figure 10: Time analysis of existing and proposed method

5 CONCLUSION

In this paper, high-performance VLSI architectures for lifting based 2D-DWTs are proposed. The proposed architecture Used for reducing the power and time compared to the existing architecture. The proposed and existing 2D lifting based DWTs are implemented with 45 nm technology. The results show that the proposed designs achieve significant improvement compared with existing architectures. In future, it will be implemented in FPGA Vertex kit.

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