MODERNIZED PWM TECHNIQUE FOR MODIFIED CASCADE MULTILEVEL INVERTER TO MINIMIZE THD

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Abstract

The applications of Multilevel Inverter (MLI) are increasing day by day in high power industries because of their ability to reduce output voltage harmonics [1]. Several research and studies are going on for effective control of these inverters. This paper proposes a 15 level modified cascaded MLI controlled by a modernized PWM technique. The conventional pwm technique produces output with more Total Harmonic Distortion (THD) for minimum level and becomes complex as the no of level increases. The proposed pwm technique produces better control over the output compared to conventional pwm technique for the
same level. Using the proposed pwm technique the output voltage level is also increased by two times compared to the conventional method. Thus by applying modernized pwm technique to modified cascaded MLI yields near sinusoidal output with THD as low as 2.29% which is well less than the IEEE STD 519.

**Key Words:** Pulse Width Modulation (PWM); cascaded multilevel inverter (MLI); total harmonic distortion (THD).

1 INTRODUCTION

The multi-level inverters have drawn tremendous interest in the power industry because of its ability to produce high power with medium voltage. The biggest advantage of MLI is that it is free from EMI. So implementation and maintenance of MLI is easy. The output of MLI will be with different voltage levels. As the number of voltage levels increase, the harmonic content of output voltage decreases significantly. The multilevel voltage source inverters unique structure allows them to reach high voltages and power levels without the use of transformers. There are different topologies of multilevel inverter that are used for the better control of converter output. The first topology is diode clamped multilevel inverter [2], [3], [22]. In this topology the stepped wave output is produced but with complex control. For n level inverter it requires n-1 switch pairs and capacitors. This leads to significant increase in the switching loss of the converter. The next topology is the flying capacitor multilevel inverter, here capacitors are used for splitting the voltage level in the converter. The drawback of using this topology is that there will be voltage imbalance across each capacitor which may cause distortion in the output. The commonly used topology is the cascaded multilevel inverter because of its advantages such as low EMI, less THD, reduced voltage stress (dv/dt) on the switches etc [4]. This topology has better control over the output but with the increase in level, the no of switches doubles. So the switching loss increases and with the increase in each level the no of dc sources also increases, this adds to the cost. To have better controlling capability and to have low switching loss a modified cascaded topology is used. It uses 1 capacitor for
11-level inverter, 2 capacitors for 15-level inverter, 3 capacitors for 19-level inverter and so on. In this topology we use 2 capacitors, 1 dc source and 12 switches for producing 15 level output, whereas the conventional cascaded MLI has 7 dc sources and 28 switches for producing 15 level output. So by using, modified topology the no of dc source and switches can be effectively reduced which minimizes the cost. For getting better THD at the output appropriate PWM technique has to be chosen. The modernized PWM technique is the best method for producing output with better THD. In modernized pwm technique the lower order harmonics are greatly reduced by providing low switching pulse. The modernized pwm technique is similar to that of modified sine pwm but is more effective in reducing the lower order harmonics. Thus, when the proposed PWM technique is applied to the modified cascaded multilevel inverter, a near sinusoidal output waveform can be obtained, with increased voltage level and reduced THD [24].

Figure 1 Circuit diagram of modified cascaded multilevel inverter
2 SYSTEM DESCRIPTION

Multilevel Inverters are the modification of basic bridge inverters. They are normally connected in series to form stack of level. For a conventional 7 level inverter [5]-[6] there are 3 legs and each leg has 4 switch pairs. Each leg will be supplied using separate dc sources. But for a modified cascaded inverter there will be only one dc source for any no of levels. With the help of modified PWM technique the no of levels can be increased to 2n+1. So for the modified topology with the help of modernized PWM technique the no of levels can be increased to 15. One biggest advantage is that with a single dc source the output voltage magnitude can be increased greater than the input voltage. So for a 15 level modified cascaded H-bridge inverter the number of legs needed are 3 and the switching pairs needed are 12.

Fig. 1 shows the circuit diagram of the modified cascaded multilevel inverter. The diodes are used as a return path. Only with the help of diodes the cycle completes. In the three legs 6 switches are used for positive half cycle and 6 switches are used for negative half cycle. The different voltage levels that can be obtained using the modified topology are 0, 0.25VDC, 0.5VDC, 0.75VDC, VDC, 1.25VDC, 1.5VDC, 1.75VDC. So with the help of the proposed topology the output voltage can be nearly increased to twice the supply voltage. By properly manipulating the pulses, the different voltage levels can be reached. For each level different switches are turned on and off. The switching patterns of the modernized PWM technique applied to modified cascaded multilevel inverter is described in the Table 1.
The switching pattern shows that only minimum of 4 switches and maximum of 6 switches are ON during any level of output, thus minimizing the switching losses to a greater extent. The modernized PWM technique helps greatly in minimizing the switching loss as well as the lower order harmonics. Switches S1 and S4 pairs are used for positive half cycle and S2 and S3 pairs are used for negative half cycle. S1 pair is continuously turned on during the positive half cycle whereas S4 pair is manipulated to get the different voltage levels in the positive half cycle. Similarly S2 pair is turned on during the entire course of negative half cycle and S3 pair is manipulated to get the required voltage levels which is clearly shown in Table. 1.

### 3 Simulation Results

Simulation was carried out for a modified 15 level cascaded MLI that comprises of 12 switches powered by a single DC voltage source. The proposed topology was obtained by cascading three H-bridge structures in which the first bridge is powered by DC voltage and rest of the bridges are supplied through two individual capacitors as shown in Fig. 1. The switching sequence are calculated using modernized PWM technique which is shown in Table. 1. MATLAB Simulink tool was used to simulate the proposed topology. The simulation is performed considering the practical values.
by properly setting the snubber resistance and capacitance value.

A. Pulse Pattern:

The results shown in Fig. 2 portrays the positive pulse pattern obtained across switches with a magnitude of 1V and time period of 20ms. The switches S1, S11, S12 are continuously turned on during the entire positive half cycle which can be clearly seen from Fig. 2. The switch S4 is turned on to get the higher level output. This is continuously turned on from VDC to 7VDC/4 which helps in minimizing the switching loss. Where as S41 and S42 are used for reducing the lower order harmonics.

![Time Series Plot: Positive Pulse](image-url)

Figure 2 Positive pulse pattern

The negative sequence pulses are shown in Fig. 3 which is in complementary to the positive sequence obtained across each switch. Similar to positive half cycle the switches S2, S21 and S22 are continuously turned on during the entire negative half cycle. The switch S3 is turned on for higher level outputs in negative half cycle S31 for medium level outputs and S32 for lower level outputs. The remaining two switches are used for reducing the lower order harmonics which helps in getting a better output.
B. Output waveforms:

Fig. 4 shows the output voltage of 15-level modified cascaded MLI which is nearly sinusoidal. The output voltage waveform is compared with the reference sinusoidal voltage for clear perspective. The comparison is shown in Fig. 5 which clearly portrays that the deviation obtained from the modernized PWM technique is very minimal. As the modified topology is asymmetrical the output obtained is having more levels. The given input voltage is 192V and the peak output is 336V, which cannot be obtained using a symmetrical topology.
From Fig. 6 we can clearly see that the voltage THD is 2.29%. Thus the proposed system with the modified PWM technique provides output with better THD. So the proposed system can be used where better performance is expected.
4 CONCLUSION

Multilevel inverters are generally used for high power applications with better resolution in their output waveform. The biggest advantage of using this topology is that the voltage level is increased nearly twice compared to the conventional method at reduced cost. From the results it is clearly evident that with the application of modernized pwm technique the output voltage distortion is very less with a THD of 2.29%. The only constraint is that there will be a voltage imbalance across the capacitors. In future this problem can be rectified by using a suitable technique which helps in the improved performance of the converter [23]. The proposed work can be further extended with increased voltage levels for industrial applications. Furthermore, the modified cascaded MLI can be a suitable interconnection between the renewable energy sources connected to smart grids or other standalone applications.

References


