

Design and Analysis of Low Power Braun Multiplier Architecture

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Abstract— In recent years, power dissipation is one of the biggest challenges in VLSI design. Multipliers are the main sources of power dissipation in DSP blocks. Power optimization has to be implemented on all components of the processor. In this paper, the design and power comparison of the low power unsigned array multipliers using different types of adder units are analyzed. The fundamental units to design a multiplier are adders. The proposed multiplier is designed by using different types of full adder and half adder units. The design of full adder and half adder for low power is obtained and the low power units are implemented on the proposed multiplier and the results are analyzed for better performance. The designs are done using TANNER SEDIT tool and are simulated using TSPICE. The experimental tanner SPICE results show that the transistor count and the power required are significantly reduced in the proposed design over the existing design.

Key terms: BRAUN multiplier, unsigned multiplication algorithm, full swing 16T full adder, SERF full adder, 12T XOR.

INTRODUCTION

Very Large Scale Integrated (VLSI) circuit technology is the rapid growing technology for a wide range of innovative devices and systems that have changed the world today. In the past, the major concerns of the VLSI designer were area, performance, cost and reliability. Power was mostly of only secondary importance. Now adays, however, this trend has changed a lot, power is given primary importance than area and speed. The explosive growth in laptop and portable systems and in cellular networks has intensified the research efforts in

low power electronics. High power systems often may lead to damage several circuit damages. Low power

leads to smaller power supplies and less expensive batteries.

The multiplier circuit is a core component of most of the present day digital signal processors. Therefore, the demand for multiplier-performance improvement is increasing. Multipliers are a major source of power dissipation. Reducing the power dissipation of multipliers is key to satisfying the overall power budget of various digital circuits and systems.

In this paper, power reduction for unsigned multipliers is explained and power comparisons of BRAUN multipliers are obtained. For power reduction the AND gates are replaced with NOR gates. The half adder units are also modified in the proposed design for the excellent reduction in both the power and transistor count. This paper is organized as follows: In section 2 the unsigned multiplication algorithm is given. Section 3 deals with the existing/ conventional array multiplier architecture .In section 4 the designs of different adders are discussed. Section 5 the proposed multiplier design is described. Section 6 experimental results and conclusion are discussed, which validate the proposed method.

UNSIGNED MULTIPLICATION ALGORITHM

Utilizing AND gates and full adders, multiplication can be implemented on the processor in the same way as it is done by hand: multiply each digit of the multiplier by the multiplicand, thereby generating partial products and

$$X = \sum_{i=0}^{n-1} X_i 2^i$$

then sum up the respective partial products in order to generate the final result. Assume that X and Y are two n-bit unsigned numbers, where X is the multiplicand and Y is the multiplier. They can be expressed as follows:

(1)

$$Y = \sum_{j=0}^{n-1} Y_j 2^j \quad (2)$$

The product of X and Y is P and it can be written in the following form:

$$P = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} X_i Y_j 2^{(i+j)} \quad (3)$$

Each of the partial product terms $P_n = X_i Y_j$ is called the summand. All the partial products then get added up to generate the final product [7].

1. EXISTING ARCHITECTURE

Array multipliers are high speed parallel multipliers. Unsigned array multipliers are also known as Braun multipliers or Carry Save Array Multipliers [7][8]. This multiplier is restricted to performing multiplication of two unsigned numbers. It consists of an array of AND gates and adders arranged in an iterative structure that does not require logic registers. This is also known as the non-additive multiplier since it does not add an additional operand to the result of the multiplication. Architecture of a n*n bit multiplier requires n(n-1) and n^2 AND gates.

Each of the $X_i Y_j$ product bits is generated in parallel with the AND gates. Each partial product can be added to the previous sum of partial products by using a row of adders. There is no horizontal propagation of carry. The braun multiplier performs well for unsigned operands that are less than 16 bits. The conventional unsigned array multiplier architecture is given in figure 1.

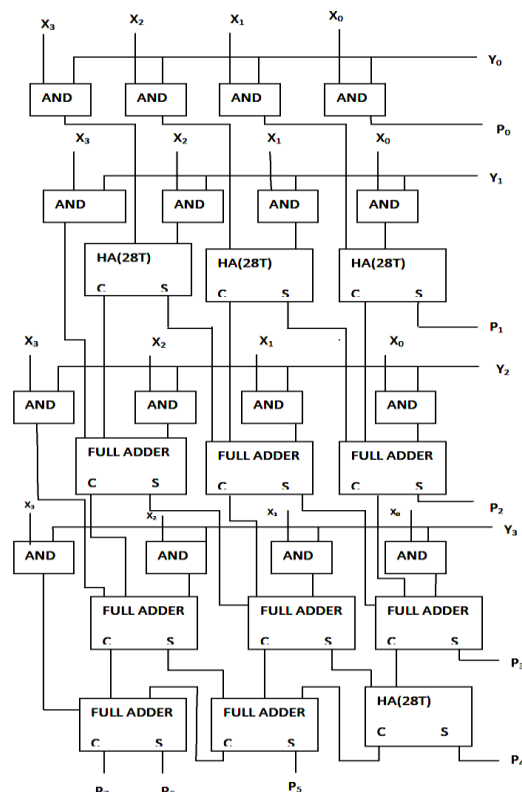


Figure 1. Conventional unsigned array multiplier

The half adders used in the existing multiplier is the 28transistor conventional CMOS adder. The design of conventional XOR gate of 22T and the conventional half adder of 28T, that are used in the existing array multiplier are given in figure 2 and figure 3 respectively.

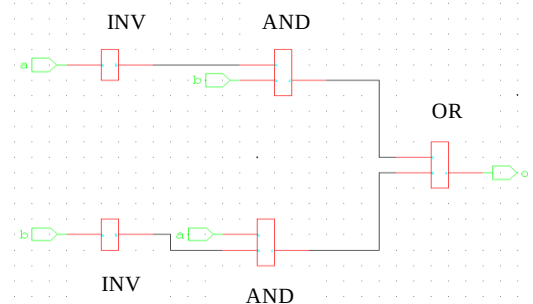


Figure 2. XOR gate (22T)

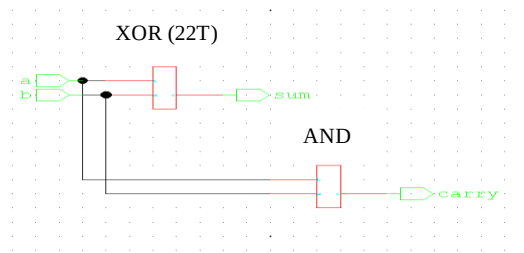


Figure 3. Conventional half adder(28T)

DESIGN OF FULL ADDERS

The existing and proposed array multiplier will be designed and power analyzed for different full adders like CMOS normal full adder, 16 transistor full adder, 14 transistor full adder and SERF 10 transistor full adder and from the comparison the power optimized multiplier will be found out.

Four different full adders are used for analysis. The first one is the normal CMOS full adder[8] in figure 4 which is having 62 transistors.

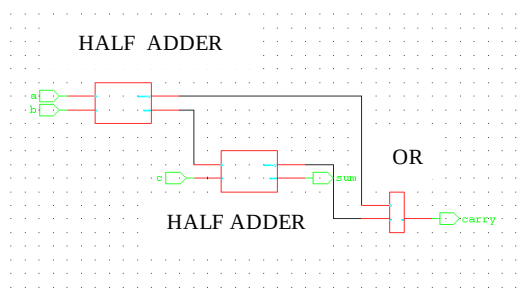


Figure 4. CMOS full adder (62 T)

The second full adder is the 16T full adder [4] which is having full swing and is having low power consumption than the transmission function adder [2][3] is shown in figure 5.

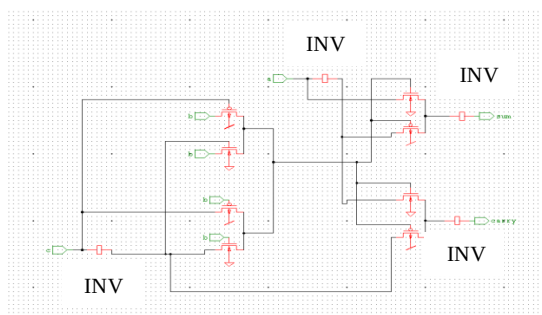


Figure 5. Full swing 16T full adder

A Novel 14T full adder[5] is the next full adder used for the analysis and is better than the conventional 14T [7] in the figure 6.

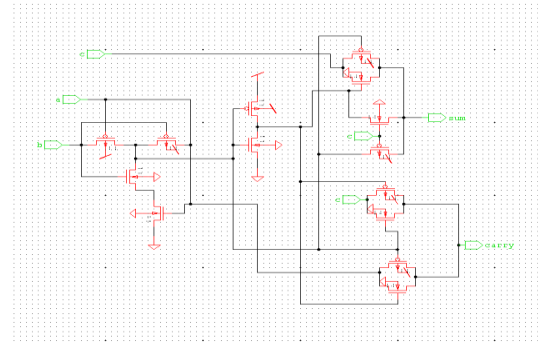


Figure 6. New 14T full adder

Static energy recovery full adder [6] is the fourth one which is having 10T and it is having low power than the conventional 10T full adder[7] is shown in the figure 7.

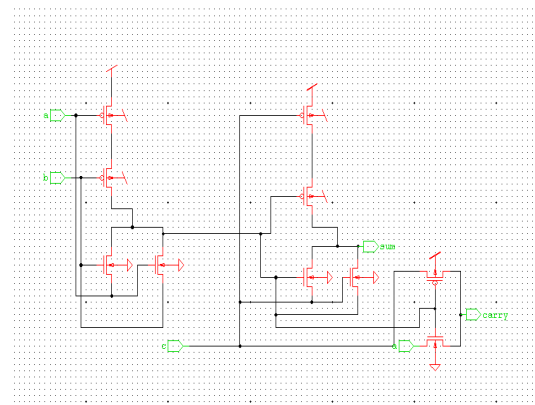


Figure 7. SERF full adder

PROPOSED ARCHITECTURE

The process of array multiplication which follows the unsigned algorithm, is the AND operation of multiplicand and multiplier bits and its followed addition. The AND gates in the conventional multiplier are replaced with NOR gates in the proposed multiplier [1], according to the DeMorgan's Law:

$$A.B = (A'+B')' \quad (4)$$

From (4) its clear that the inputs have to be complemented. AND gates have 6 transistors but NOR gates have 4 transistors. For a 4*4 multiplier 8 inverters are initially required, 16 AND gates are replaced with 16 NOR gates, thus in total when compared to conventional 16 transistors are saved in existing multiplier. The proposed design of unsigned array multiplier is given in figure 8.

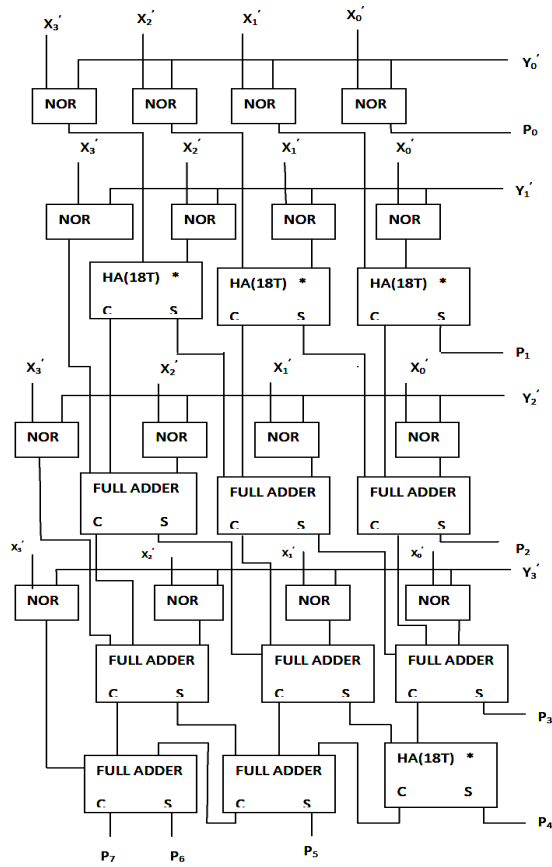


Figure 8. Proposed unsigned array multiplier

The half adders used in the proposed design are with 12transistor XOR gate. In the proposed multiplier again 10 transistors are saved by this modification in one half adder unit alone. The 22T XOR gate of the half adder of the existing multiplier is replaced with 12T XOR gate in the half adder of the proposed multiplier. The 12T XOR gate is given in figure9. Half adder in the proposed design is with 18T and it is having good power reduction than 28T conventional half adder. The proposed and existing array multipliers are analyzed for good power results with different full adder units.

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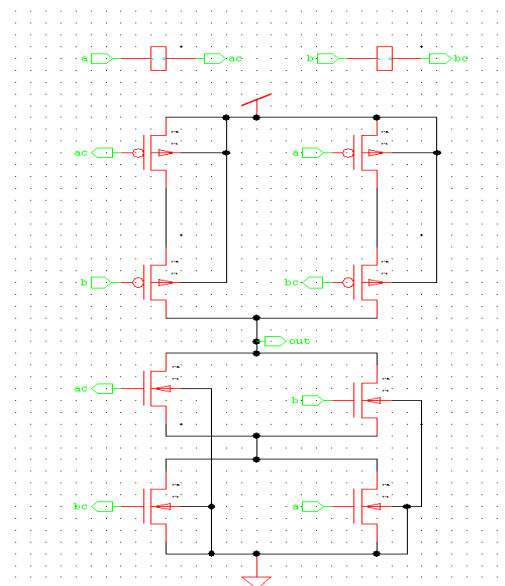


Figure 9. 12T XOR

RESULTS AND DISCUSSION

The designs are done in TANNER SEDIT 12.0 tool and the simulations are done and the power results are obtained in the TANNER TSPICE 12.0. The power comparisons of different units in the existing design and proposed designs are shown in figure 10 to figure 13 and the multiplier power comparison is given in figure 14. A table 1 showing transistor count is also obtained for existing and proposed array multipliers.

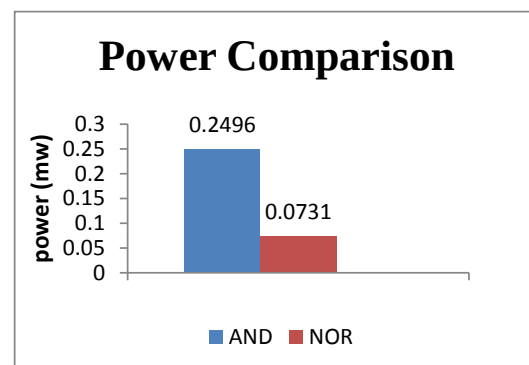


Figure 10 . Power comparison of AND(6T) gate and NOR(4T) gate

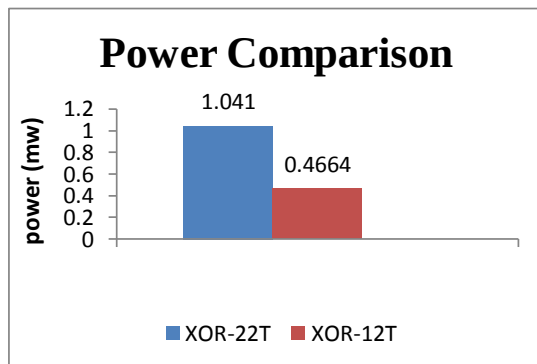


Figure 11. Power comparison of 22T XOR and 12T XOR gates

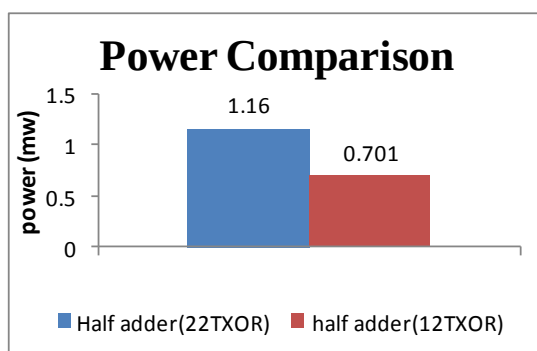


Figure 12. Power comparison of 22T XOR half adder and 12T XOR half adder

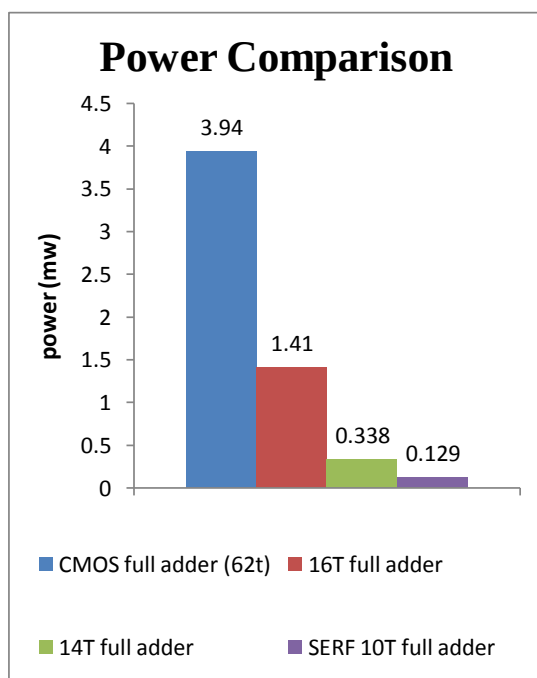


Figure 13. Power comparison of different full adders

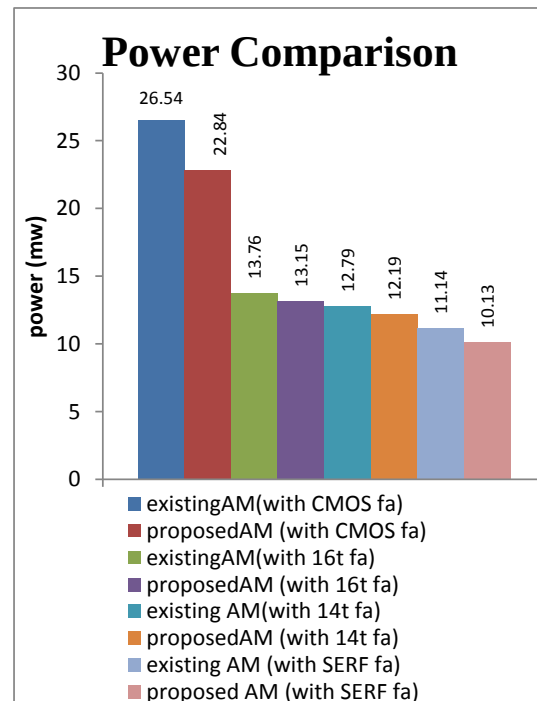


Figure 14. Power comparison of different unsigned array multipliers (AM).

TABLE 1
TRANSISTOR COUNT OF DIFFERENT ARRAY MULTIPLIERS

Array multiplier(AM)	No.of transistor count
Existing AM (with CMOS fa)	704
Proposed AM (with CMOS fa)	648
Existing AM (with 16Tfa)	336
Proposed AM (with 16Tfa)	280
Existing AM (with 14Tfa)	320
Proposed AM (with 14Tfa)	264
Existing AM (with SERF fa)	288
Proposed AM (with SERF fa)	232

CONCLUSION

The existing and proposed array multipliers are designed using TANNER sedit tool and the power results are analysed with different adder units using Tspice. It is therefore found that the proposed array multipliers have transistor count and power range less than that of existing multipliers. Proposed Multipliers with the CMOS full adder have 8% reduction in transistor count and about 13.9% power reuction than the existing multiplier with CMOS full adder.

Multipliers with 16T full adder have 16% transistor count reduction and 4.4% power reduction in the proposed than the existing. Transistor count reduction and power reduction are 17.5% and 4.6% respectively for the proposed multiplier with 14T full adder than the existing multiplier with 14T full adder. Finally the proposed multipliers with SERF have 19.4% reduction in transistor count and 9% power reduction than the existing multiplier. Therefore it is found that the proposed multiplier with SERF have better results than the other multipliers.

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