



Comparison of Low Power 2-stage Delay Buffers with various Base Cells

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Abstract

In the past few decades, recent studies have demonstrated that the power dissipation in the Information and Communication Technology (ICT) devices is a big challenge while designing. The memory storage elements, the logic elements and the clocking distribution are the main sources of power dissipation and the consumption. This paper presents a dual dynamic node pulsed hybrid buffer (DDB). The development, implementation and the testing of this low power buffer are described in this paper. Buffers are accessed in the form of ring counter. Buffer controls the data transfer between the chips in the computer internal circuits. The slew rate is control by the C-Element. There is an improvement of 44.08 % and 14.20 % for the 2-stage buffer with fixed biased and SRAM cells in the power dissipation respectively.

Key Words and Phrases: ICT, DDB, buffer, C-Element, Slew Rate.

1 Introduction

Power dissipation on buffer constitutes a major amount of the total power consumption in the computer, since the buffers are responsible for various switching activities. And flip flop is also the main components in all the buffer. Reducing the power dissipation in the flip flop is a challenge nowadays. Because of this effects, whenever electronic devices are used for prolonged time, they become heated. Even there can be blast due to heating effect. Even in computers, the buffers are used in various circuits. Examples can be given as in generating data address, data transmission with delays, etc. When the same data or the same address is going to be transmitted or generated, there are unnecessary switching activities occurring. These activities will increase the power dissipation. And they also contribute in the overall power consumption of the computer.

With technology scaling, the low power design in Information and Communication Technology (ICT) devices emerged as a challenging research in todays electronics world. The delay buffer uses several new techniques to reduce the power consumption. One of the crucial factors that helps in reducing the power dissipation is the proper flip flop utilities with a proper clock distribution network. In many portable electronic products, delay buffer (synchronizer) is used as a significant portion of their circuits. And such serial access memory using buffer is needed in temporary storage of signals. Most circuits adopt Static Random Access Memory (SRAM) as discussed in Ref. [1] in addition of some control/addressing logic to implement delay buffers. Decoders in SRAM uses flip flops as well. Buffer is also used as word line driver for driving large capacitive loads. It reduces the power dissipation and the propagation delays by avoiding the redundant events.

A Ring Counter is used to monitor the data loading. Ref. [2] proposed that the ring counter can be assembled by an array of Flip Flops triggered by a global clock signal. Such a gated Ring Counter is also used to compose a low power First in First out (FIFO) memory cells. For this, double edge triggered flip flops (DETFF) had been used. It uses both the edges (rising and falling edges) for triggering the flip flop.

Recently many researchers have been investigating about the sources of power dissipation in the electronic devices. There are various ar-

issues which contribute in the power dissipation in Very Large Scale Integrated Circuit (VLSI) designs. They are computer related and electrical related issues. Computer related issues are in the designs of buffer, clock signaling, address decoder circuit, pulse generator for Read only Memory (ROM), etc. And the electrical related issues are interconnects, crosstalk, coupling effects, delays, transient characteristics, etc.

The interconnects and the clock distribution system consumed about 20 %-40 % of the total power as stated by [3]. So the first priority was given to global clock distribution system in this research work. Since flip flops are the core components in designing any VLSI circuits, a novel approach to reduce the gated clock levels with various several different Flip Flop topologies were also studied. This will avoid the loading effects of the global clock signal. This technique will considerably decrease the loading on distribution network of the clock signal for the ring counter and thus the overall power consumption. The Octree clock distribution system will be used to reduce the gated clock levels.

In most VLSI devices, the clock network and clocked data elements are the main sources of power dissipation. In the elements such as buffer, when there are switching activities in their internal capacitance, they result in more power dissipation. This may happen with every clock transition/pulse into the sequential element. Ref. [4] explicated that by increasing the clock interconnection capacitance, the clock voltage swing can be reduced. But the sequential elements can retain their state and their output the same, before and after the clock pulse; when they are expected to change. This contributes in unnecessary dissipation of power due to clock transition. Power dissipation can be minimized by designing the buffer in such a way that they can gate the clock and use the clock when needed. In the proposed design, triggering is done based on the non-redundant events. It avoids the redundant events and thus reduces the unwanted switching activities. Even the data path is reduced with the employment of the Octree clocking distribution system, since with one input there will be eight fan-outs in a cycle. This investigation on low power applications of buffer will help the ICT markets to expand in more reliable way in the future in terms of power consumption. Specially while designing computer and other electronic devices, the power consumption will be reduced and they

can be used for long time with very less heating effects.

2 Dual Dynamic Node Pulsed Hybrid Buffer

In this type of Buffer, Dual dynamic node pulsed hybrid flip flop (DDFF) is employed. The output of the pull-up and pull-down transistors are driven by the precharge node. So it has large precharge capacitance [5] [6]. The circuit diagram is given in figure 1.

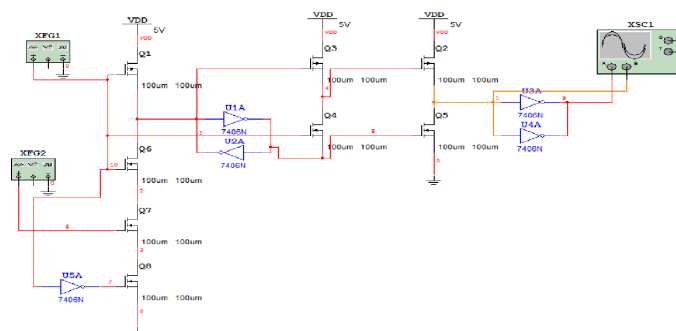


Figure 1: Circuit diagram of Dual dynamic node pulsed hybrid (DDB).

It operates in two modes: evaluation phase (when clock is high) and precharge phase (when clock is low). It reduces the redundant events and also the pipeline overhead. It has unconditionally shut off mechanism and provide the clock signal only when it is required. The simulation is shown in figure 2. The Octree clocking system is employed with this design to reduce the loading effects in the buffer. The employment of Octree system is justified in Table 1.

In figure 2, it is observed that the output is produced faithfully with an introduction of delay. The power dissipation for this buffer is 1.655 nW in 2-stage.

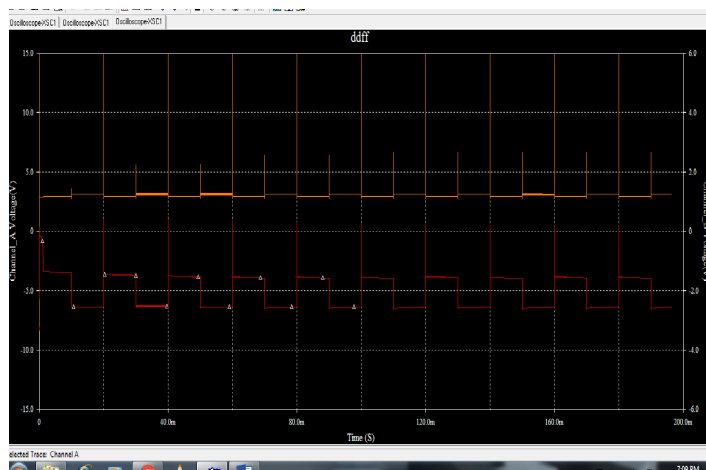


Figure 2: Simulation of DDFF.

3 Comparison of Power Dissipation

Power analysis of the delay buffer at 2.25V, 568 MHz with the time scale of 5ns in CMOS 90nm using the Octree system is given below. It is compared with the Quad clock distribution system.

Table 1: Power Analysis (@Time Scale 5ns, 64 bits)

Structure	Quad System(mW)	Octree System(mW)	Percentage of Improvement
Delay Buffer for 64 bits	0.768	0.666	13.28

For a single stage buffer, only one DDFF is used with the global clock distribution system. In this case, the power dissipation remains same as that of DDFF. The comparative analysis and discussion of the power dissipation in the low power buffer designs is given below in table II.

The above figure 3 and figure 4 show the circuit diagrams of Fixed Body biased Buffer and SRAM based Buffer respectively.

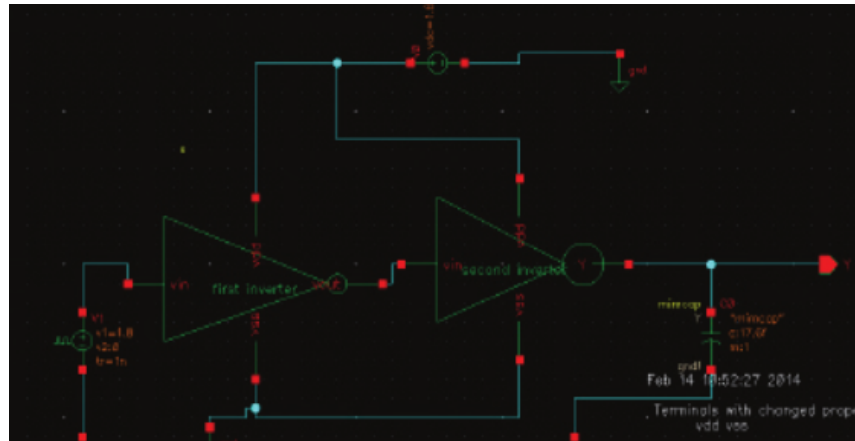


Figure 3: Circuit diagram of Fixed Body biased Buffer.

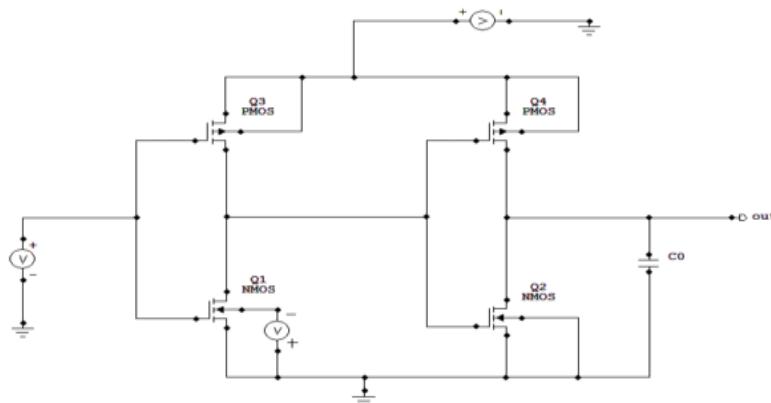


Figure 4: Circuit diagram of SRAM based Buffer.

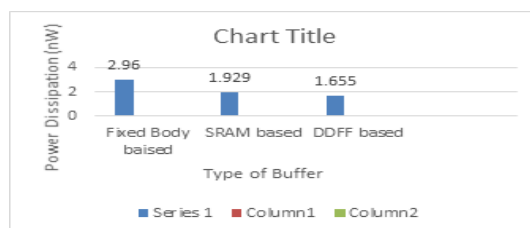
These works were done by the respective references as shown in the Table 2. The power analysis of the buffers are done for 2-stage buffer designs.

Table 2: Power Analysis of 2-stage Buffer

Reference	Flip Flop Used	Power Dissipation(nW)	Percentage of Improvement
[7]	Fixed Body Biased	2.96	44.08
[8]	SRAM	1.929	14.20
Proposed Work	DDFF	1.655	—

4 Analysis Graph of Power Dissipation

The following figure 3 shows the analysis of power dissipation in the graphical form



This low power buffer will be a new revolution in the digital designs. With this the power consumption and dissipation will be reduced a lot. It can be observed that the switching occurs only in the data line where the redundant events are avoided.

5 Results and Analysis

Thus an optimal DDB is presented with Octree clocking distribution. The DDB circuit is simulated using Multisim with power

dissipation of 1.655 nW. The Comparative power dissipation analysis is given in Table 2. It is done in the normal condition of 5V and 27C.

6 Conclusion

An optimal low power DDB is successfully used in various chips of a computer with the improvement of 44.08 % and 14.20 % for the 2-stage buffer with fixed biased and SRAM cells in the power dissipation respectively. DDB has lesser switching activities as it avoids redundant events and thus has very low power dissipation.

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