



An Improved Design of a Reversible Fault Tolerant Encoder Based FPGA

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Abstract— Irreversible circuits dissipates heat to reload lost information because of overlapped mapping between input and output vectors. Fault Tolerant reversible encoders are the imperatives of the topnotch computing systems. This paper presents the design of reversible fault tolerant architecture of encoder with minimum quantum cost. A new 4*4 fault tolerant reversible gate is proposed for designing efficient reversible fault tolerant 4*2 and 8*3 encoders. In addition, an optimized reversible fault tolerant 2*2 Vedic multiplier has been proposed by using new cost effective gates. Besides, the design of the proposed logic elements procures lower bounds in the number of gates compared to the existing design. Furthermore, the proposed design improves upon the best known existing designs in terms of quantum cost and unit delay. Finally, the proposed gate finds its application in 4*4 fault tolerant Vedic multiplier.

Keywords— *Fault Tolerant; Reversible Logic; Quantum Cost; Garbage output; Vedic Multiplier*

I. INTRODUCTION

With the advancement of technology, integration at higher level and employment of fabrication technique has astoundingly reduced the energy loss in the past decades. Thereupon, optimized low power hardware computations have become a salient area of research. As stated by R. Landauer [1], information bits when lost dissipates $n \cdot (k \cdot T \cdot \ln 2)$ joules of energy where n is the summation of the information lost, k is Boltzman constant, T is absolute temperature. In the early 1970, C.H. Benett's research [2] proved that with the aid of reversible logic gates the huge energy dissipation due to lost information bit can be circumvented. Fault tolerance indicates the property that enables a system to continue its intended operation instead of failing completely due to one or more faults within. Conventionally, FPGA comprehends an array of configurable logic block connected via programmable interconnects. FPGAs can be reprogrammed as required for desired applications.

The method of multiplication consists of formation of partial product, addition of partial product and eventually product is procured. Accordingly, the consummation of Vedic multiplier[7] involves number of steps which includes "vertical

and crosswise" multiplication process to upgrade the speed of the operation.

The paper is systematized as follows; Section 2 provides comprehension of reversible logic design and fault tolerance property. Improved design of reversible fault tolerant 4*2 Encoder as well as 8*3 Encoder is illustrated in section 3. In section 4, an application of the proposed gate is elucidated by the implementation of reversible fault tolerant 2*2 Vedic multiplier as well as 4*4 reversible fault tolerant Vedic multiplier. Section 5 propounds the simulated and analyzed result. Finally, the paper is concluded in the last section.

II. BASIC DEFINITIONS AND LITERATURE REVIEW

In this section, the basic definition of reversible fault tolerant gate, garbage output, quantum cost, unit delay, constant input and gate count are proffered.

A **reversible gate** consists of an n input lines I_n and n output lines O_n , forming $n \times n$ data stripe block that generates a unique mapping of output pattern with each possible input pattern $I_n \leftrightarrow O_n$.

A **fault tolerant gate** is a reversible gate which is parity preserving if the parity of the input and output vectors are maintained as $I_1 \oplus I_2 \oplus \dots \oplus I_n = O_1 \oplus O_2 \oplus \dots \oplus O_n$. In this paper, the parity of the proposed gate is preserved with the aid of fault tolerant gates which detects the occurrence of faults.

The **quantum cost (QC)** can be obtained by substituting the reversible gates of a circuit with primitive quantum gates. It is referred as the cost of the reversible circuit in terms of the cost of elementary gates. The quantum cost for 1*1 and 2*2 reversible gates are 0 and 1, respectively.

Different types of reversible fault tolerant gates are given as:

- A. **Feynman Double Gate (F2G)** : Feynman Double Gate[4] is a 3*3 reversible gate which has A, B and C as inputs and its corresponding outputs are P, Q and R. This gate has quantum cost 2.

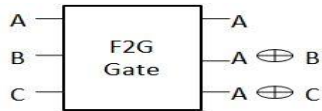


Fig. 1 Feynman Double Gate

- B. **Fredkin Gate (FRG)** : Fredkin gate[3] is a 3*3 reversible fault tolerant gate having quantum cost of 5.

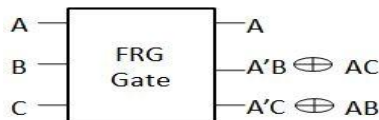


Fig. 2 Fredkin Gate

- C. **Modified New Fault Tolerant Gate (MNFT)** : New Fault Tolerant Gate[5] shows a 3*3 gate which combines XOR gate, NOT gate and AND gate having input as A, B and C while output as P, Q and R. The quantum cost of this gate is 5.

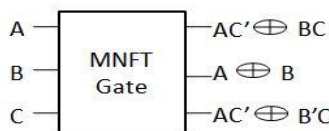


Fig.3 Modified New Fault Tolerant Gate

- D. **Islam Gate (IG)**: Islam gate[6] is a 4*4 reversible gate. Quantum cost of Islam gate is 7.

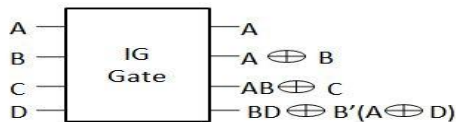


Fig. 4 Islam Gate

Some of the reversible logic gates as shown above are used in the proposed design.

Garbage Output (GO) stipulates the outputs that are unused in the circuit which cannot be shunned as it is required to achieve reversibility. A circuit should contain less number of garbage outputs.

Gate Counts (GC) refers to the number of reversible gates that are used for the designing of the circuit, so as to keep it minimum.

Constant Inputs indicates the number of inputs that are to be kept constant at either 0 or 1 with the aim of compounding the logical function.

III. PROPOSED REVERSIBLE FAULT TOLERANT DESIGN

This section exemplifies the design layout, theoretical properties and working principle of the proposed design used in 4*4 Reversible Fault Tolerant Vedic multiplier.

A. Proposed Reversible Fault Tolerant Gate

We propose a new reversible fault tolerant gate together with its block diagram, quantum cost and truth table.

1) **GJ (Gopal-Jyotsna) Gate**: Fig. 5(a) and 5(b) indicates the proposed GJ gate with its quantum realization. It is a 3*3 reversible fault tolerant gate. The GJ gate can be described as : $I_v = (A, B, C, D)$; $O_v = (A, A'B \oplus AC', AB' \oplus A'C, D)$, where I_v and O_v are the input and output vectors respectively. Quantum Cost of GJ gate is five. This gate forms a reversible fault tolerant 4*2 Encoder.

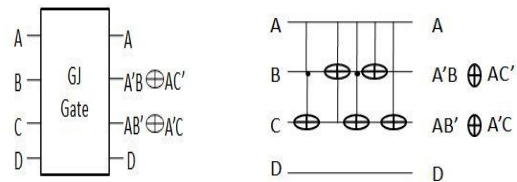


Fig.5 GJ Gate (a) Block Diagram (b) Quantum Realization

B. Fault Tolerance Property of Proposed Gate:

Table I corroborates the unique one to one mapping and parity preservice between input (A, B, C and D) and output (P, Q, R and S) of the proposed GJ gate. For any input combination, corresponding output combination indicates the same parity ($A \oplus B \oplus C \oplus D = P \oplus Q \oplus R \oplus S$) as well as reversibility of the proposed gate.

Table II shows the truth table of the reversible fault tolerant 4*2 Encoder.

TABLE I
TRUTH TABLE OF PROPOSED GJ GATE

INPUT				OUTPUT				PARITY 1=ODD, 0=EVEN
A	B	C	D	P	Q	R	S	
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	1
0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	0	0	1
0	1	0	1	0	1	0	1	0
0	1	1	0	0	1	1	0	0
0	1	1	1	0	1	1	1	1
1	0	0	0	1	1	1	0	1
1	0	0	1	1	1	1	1	0
1	0	1	0	1	0	1	0	0
1	0	1	1	1	0	1	1	1
1	1	0	0	1	1	0	0	0
1	1	0	1	1	1	0	1	1
1	1	1	0	1	0	0	0	1
1	1	1	1	1	0	0	1	0

TABLE II

TRUTH TABLE OF REVERSIBLE FAULT TOLERANT 4*2 ENCODER

INPUT				OUTPUT	
A	B	C	D	Y1	Y2
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

C. Proposed Reversible Fault Tolerant 8*3 Encoder

The hardware realization of 8*3 encoder which is designed using reversible fault tolerant gates is shown in fig.6. The reversible gates used for the implementation of the encoder are the proposed GJ gates and Double Feynman gates. The circuit requires a total of 5 reversible fault tolerant gates which comprises of 3 Double Feynman gates and 2 GJ gates. The quantum cost of the proposed 8*3 encoder is enumerated to be 16. The total number of garbage outputs is 5.

The truth table for the proposed 8*3 Encoder clarifies the validity of the design. Table III shows the encoded output for the corresponding inputs.

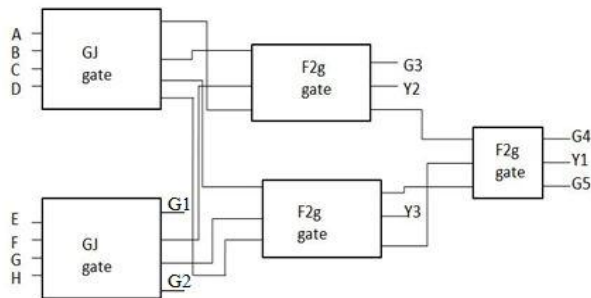


Fig. 6 8*3 Encoder Block Diagram

TABLE III

TRUTH TABLE OF 8*3 REVERSIBLE FAULT TOLERANT ENCODER

INPUT								OUTPUT		
A	B	C	D	E	F	G	H	Y1	Y2	Y3
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

IV. APPLICATION OF THE PROPOSED DESIGN TO IMPLEMENT A 4*4 REVERSIBLE FAULT TOLERANT VEDIC MULTIPLIER

A. Proposed Reversible Fault Tolerant 2*2 Vedic Multiplier

Fig. 7 shows the architecture of proposed reversible fault tolerant 2*2 Vedic Multiplier to produce the desired output with 9 garbage values and 7 constant outputs. The architecture uses two GJ gates, one MNFT gate, three F2G gates, one FRG gate and one IG gate.

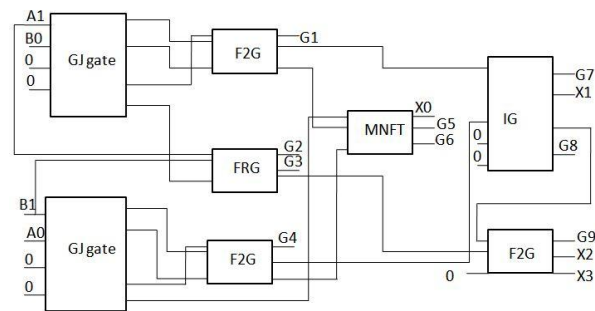


Fig. 7 Reversible Fault Tolerant 2*2 Vedic Multiplier

The expressions to obtain the output for the 2*2 Vedic Multiplier are:

$$X0 = A0.B0$$

$$X1 = A1.B0 \oplus A0.B1$$

$$X2 = A0.A1.B0.B1 \oplus A1.B1$$

$$X3 = A0.A1.B0.B1$$

TABLE IV

TRUTH TABLE OF REVERSIBLE FAULT TOLERANT 2*2 VEDIC MULTIPLIER

INPUT				OUTPUT			
A0	A1	B0	B1	P0	P1	P2	P3
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	1	1
1	1	0	1	0	1	1	0
1	1	1	0	0	1	0	0
1	1	1	1	1	0	0	1

B. Proposed Reversible Fault Tolerant 2*2 Vedic Multiplier

The 4*4 reversible fault tolerant Vedic multiplier is designed using 2*2 Vedic multiplier which is also consists of reversible fault tolerant gates. The block diagram assimilates 4-bit and 6-bit reversible fault tolerant Ripple Carry Adder (RCA)[8] whose inputs are taken from the outputs of four 2*2 reversible fault tolerant Vedic multiplier. The RCAs are formed with the assistance of fault tolerant full adder (FTFA). The architecture of the 4*4 Vedic multiplier is shown in fig.8.

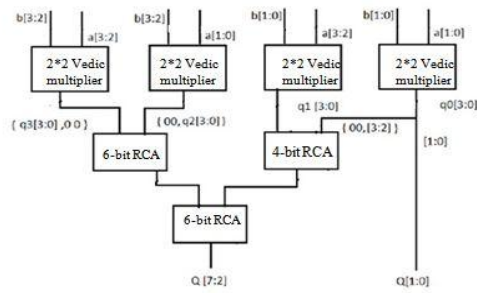


Fig. 8 Reversible Fault Tolerant 4*4 Vedic Multiplier

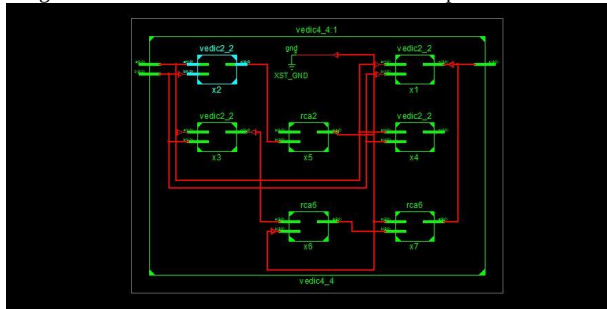


Fig.9 Design of Reversible Fault Tolerant 4*4 Vedic Multiplier

V. SIMULATION RESULT

The simulated outcome indicates that the proposed circuits give correct output for all combinations of inputs. The simulation of the proposed architecture is done using Xilinx 13.1 software[16] and synthesized for Spartan 6-FPGA board. The result obtained on simulating the proposed design is shown in fig.10 (a), fig.10 (b) and fig.10 (c). The output of 4*4 Vedic Multiplier is shown in fig.13 where the inputs are given as, multiplier a = "15" and multiplicand b = "15" so, the result shows s = "225". Table V demonstrates the comparative analysis between the proposed and existing 8*3 Encoder. Thereupon, the comparison between the proposed designs of reversible fault tolerant 2*2 Vedic multiplier is done with the existing work and shown in Table VI. The proposed reversible fault tolerant 2*2 Vedic multiplier requires 8 gates, 33 quantum cost, 7 garbage outputs and 8 unit delay whereas the best known existing design require 10 gates, 50 quantum cost, 18 garbage outputs and 10 unit delay. Finally, Table VII depicts the comparative analysis of the 4*4 Vedic multiplier.

VI. FUTURE PROSPECT

The work can be extended to design the Discrete Cosine Transform for image compression systems since there have been proliferations in the area of image processing in the recent years.

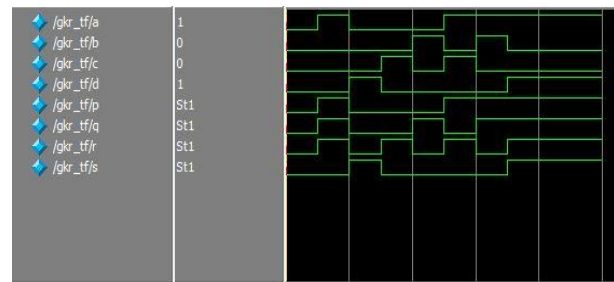


Fig. 10 (a) Simulation result of proposed reversible fault tolerant gate

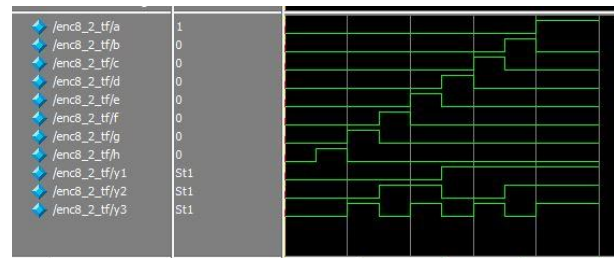


Fig.10 (b) simulation result of proposed reversible fault tolerant 8*3 Encoder



Fig.10 (c) Simulation result of Reversible Fault Tolerant 2*2 Vedic Multiplier

Name	Value	1,999,997 ps	1,999,998 ps	1,999,999 ps
s[8:0]	0111100		011100001	
a[3:0]	1111		1111	
b[3:0]	1111		1111	
q0[3:0]	1001		1001	
q1[3:0]	1001		1001	
q2[3:0]	1001		1001	
q3[3:0]	1001		1001	
temp	0010		0010	
temp	001001		001001	
temp	100100		100100	
temp	001011		001011	
q6[6:0]	0111100		0111000	
q4[4:0]	01011		01011	
q5[5:0]	101101		101101	

Fig.11 Simulation result of Reversible Fault Tolerant 4*4 Vedic Multiplier

TABLE V
COMPARATIVE ANALYSIS OF 8*3 ENCODER

8*3 Encoder	Number of Gates	Quantum Cost	Garbage Output	Unit Delay	Fault Tolerance Property
Existing[9]	11	19	5	11	No
Proposed	5	16	5	5	Yes

TABLE VI
COMPARATIVE ANALYSIS OF 2*2 VEDIC MULTIPLIER

2*2 Vedic Multiplier	Number of Gates	Quantum Cost	Garbage Output	Unit Delay	Fault Tolerance Property
Existing[10]	6	24	10	6	No
Existing[11]	6	21	9	6	No
Existing[12]	10	50	18	10	Yes
Proposed	8	33	7	8	Yes

TABLE VII
COMPARATIVE ANALYSIS OF 4*4 VEDIC MULTIPLIER

4*4 Vedic Multiplier	Path Delay(ns)	Fault Tolerant Property
Existing [13]	16.901	No
Existing [14]	15.36	No
Existing [15]	11.559	Yes
Proposed	11.354	Yes

VII. CONCLUSION

This paper presents the efficient approaches of designing reversible fault tolerant 8*3 Encoder and 2*2 Vedic multiplier. In addition, a new gate namely GJ (*Gopal-Jyotsna*) gate is presented which is reversible as well as fault tolerant having delay of 6.150ns. Finally, the design of reversible fault

tolerant 2*2 Vedic multiplier is elucidated. A design of reversible fault tolerant 4*4 Vedic multiplier is also proposed. The proposed circuits are optimized in terms of gate count, quantum cost, garbage output and unit delay. Since Vedic multiplier is an important methodology, it will be useful in many applications such as image processing systems.

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