

Analysis of Switched Capacitor Based Three Phase Quasi Switched Boost Inverter

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Abstract— In this paper, a three phase Switched Capacitor (SC) based quasi Switched Boost Inverter (qSBI) is proposed, which is based on traditional qSBI topology. Under the same operating conditions, the proposed SC based qSBI topology can provide higher boost with the lower switch stress when it is compared to other conventional qSBI-based topologies, only by adding an additional passive element like capacitor and a diode. The operating principle is explained along with the Simple Boost Pulse Width Modulation control (PWM) technique. The design of passive elements is presented and performance of the inverter topology is compared with other conventional topologies. The MATLAB/SIMULINK based simulation is carried out to validate the theoretical concepts.

Keywords— quasi Switched Boost Inverter; Switched Boost Inverter; Shoot through; Pulse Width Modulation

I. INTRODUCTION

The high performance traditional inverters like Voltage Source and Current Source Inverters (VSI and CSI) are widely used [1]-[2] in industrial applications, uninterruptable power supplies, distributed power generation, hybrid electric vehicles and renewable energy applications. Due to their bridge type structures, the traditional inverters have the issues like restricted output voltage; shoot through, misgating, electro-magnetic interference etc. The Z Source Inverter (ZSI) topology is proposed in 2002 [3] to overcome the issues and it can provide the combined performance of boost and inversion. The ZSI and its derived topologies are greatly explored from different aspects [4]-[11]. But large size of passive components can cause reduced efficiency compared to traditional converters. The switched boost inverter is proposed in [12]-[15] as an alternative for ZSI which has only one inductor and capacitor. But SBI provides discontinuous input current and offers reduced voltage gain compared to ZSI and qZSI topologies. It leads to the proposal of qSBI topology and its derivatives [16]. The qSBI can provide continuous source current with the same voltage gain offered by the qZSI topology. Even the qSBI can perform better way since it has lower number of passive components count and so it has reduced parasitic losses. Whenever high boosted voltage is used to produce increased voltage gain, the capacitor stress as well as the switch stress too becomes high. To alleviate the issues, switched capacitor is used in the dc to ac conversion [17] and dc-ac power conversion. The SC cell is used in combination with multilevel inverters to implement dc-dc boost multilevel inverters [18].

Switched capacitor cell is also used along with Z Source Inverter [19]-[20]. The switched inductor based SBI is proposed in [21]-[22]. A single phase switched capacitor based quasi SBI and the extension of n-switched capacitor cell based qSBI is proposed in [23]. It has continuous current, reduced voltage stress and shoot through current stress on the active and passive switches. In this paper, a switched capacitor based three phase quasi SBI topology is proposed and analyzed with simple boost PWM control strategy. It provides a higher voltage gain. Also an analysis is made based on the performance of the proposed topology along with the conventional ZSI, SBI, qSBI topologies.

II. THREE PHASE SWITCHED CAPACITOR BASED QUASI SWITCHED BOOST INVERTER

Fig.1 shows the three phase Switched Capacitor based qSBI (SC-qSBI) topology. It consists of a boost network and a three phase VSI. The boost network comprises of two capacitors, two diodes, one inductor and one active switch. In this structure an additional capacitor and diode are included. At the inverter terminal an LC filter is connected. The output of the inverter bridge is fed to a three phase star connected resistive load through the LC filter.

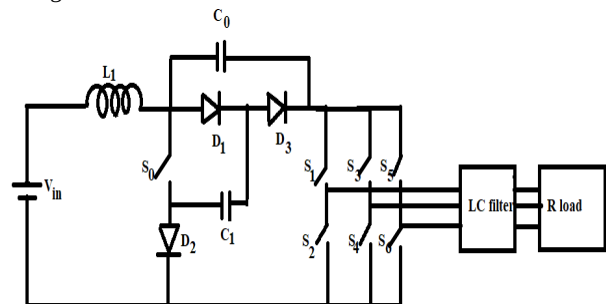


Fig.1 Three phase SC-qSBI topology

A. Modes of operation

The proposed topology has two modes of operations. One is shoot-through mode and the other one is non-shoot through mode. During shoot through mode as shown in Fig.2a, both the upper and lower switches of a single leg in the inverter circuit is switched on. During the shoot through mode, the diodes D_1 and D_2 are off, while diode D_3 is gated on. The capacitor C_1 is getting discharged while the other capacitor C_0 and the inductor

L_1 are getting charged. The time interval for this mode is DT , where D is the shoot through duty ratio and T is the switching time period. Fig. 2b shows the non-shoot through state of the inverter topology. During this mode the switch S_0 is off and the inverter can be in active state or zero state. The diodes D_1 and D_2 are on and the diode D_3 is off. The capacitor C_1 is getting charged. At the same time, the capacitor C_0 and inductor L_1 are discharged. The time duration for this mode is $(1-D)T$.

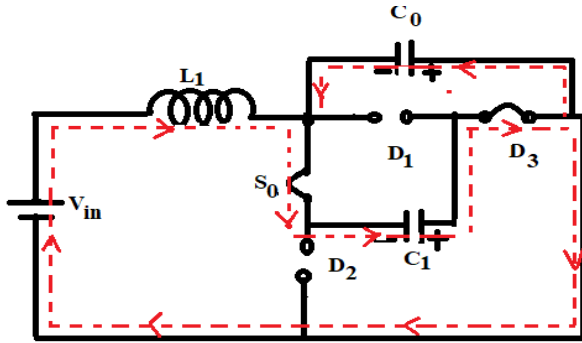


Fig.2a Shoot through mode

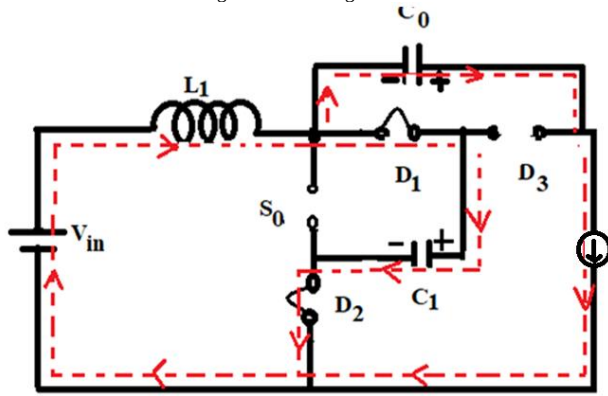


Fig.2b Non shoot through state

Fig.2 Modes of operation of three phase SC based qSBI

B. Steady state analysis of three phase SC –qSBI topology [23]

During shoot through mode, the inductor voltage is given by,

$$L_1 \frac{di_{L_1}}{dt} = V_{in} + V_{C1} \quad (1)$$

The capacitor (C_0) voltage is given by,

$$V_{C0} = V_{C1} \quad (2)$$

The peak dc link voltage (V_{PN}) is obtained as,

$$V_{PN} = 0 \quad (3)$$

The current flowing through the capacitor (C_0) is

derived as,

$$C_1 \frac{dV_{C0}}{dt} = -i_{C1} - I_{L1} \quad (4)$$

The current flowing through the capacitor (C_1) is given as,

$$C_0 \frac{dV_{C1}}{dt} = -i_{C1} \quad (5)$$

During non-shoot through state, the voltage across the inductor L_1 is given as,

$$L_1 \frac{di_{L1}}{dt} = V_{in} - V_{C1} \quad (6)$$

$$V_{PN} = V_{C0} + V_{C1} \quad (7)$$

$$C_1 \frac{dV_{C0}}{dt} = -I_{L1} - I_{PN} \quad (8)$$

I_{PN} is the peak dc link is current and is expressed by,

$$C_0 \frac{dV_{C1}}{dt} = -I_{PN} \quad (9)$$

During steady state operation, according to volt second balance, the average voltage across the inductor must be zero.

The average voltage across the capacitors are given by,

$$V_{C0} = V_{C1} = \frac{1}{1-2D} V_{in} \quad (10)$$

The peak dc link voltage is deduced as,

$$V_{PN} = V_{C0} + V_{C1} = \frac{2}{1-2D} V_{in} \quad (11)$$

The peak dc link current is given as,

$$I_{PN} = \frac{(1-D)V_{PN}}{R_l} = \frac{2(1-D)V_{in}}{(1-2D)R_l} \quad (12)$$

The instantaneous current through capacitor C_0 and the average current through the inductor are obtained as,

$$i_{C0} = \frac{2(1-D)^2 V_{in}}{D(1-2D)R_l} \quad (13)$$

Current flowing through the inductor (L_1) is given by,

$$I_{L1} = \frac{4(1-2D)^2 V_{in}}{(1-2D)^2 R_l} \quad (14)$$

The boost factor of the SC-qSBI is given as,

$$B = \frac{V_{PN}}{V_{in}} = \frac{2}{1-2D} \quad (15)$$

The peak AC load voltage per phase is given as,

$$V_{0acpk} = MBV_{in}/2 \quad (16)$$

where V_{0acpk} is the peak ac output load voltage; B is the boost factor ;M is the modulation index.

Maximum dc-ac voltage gain is obtained as,

$$G = \frac{V_{0acpk}}{V_i} = MB = \frac{M}{2M-1} \quad (17)$$

Modulation index and time period for the shoot through mode are restricted by the following constraints,

$$M = 1 - D \quad (18)$$

where D is the shoot through duty ratio

III. PULSE WIDTH MODULATION STRATEGY

The conventional modulation strategy namely Simple Boost Modulation [3] is used in this work to produce the firing pulses for the MOSFET switches. There are three modulating signals, one high frequency triangular pulse and two envelopes (one is positive and the other is negative) are used. As in the conventional Sinusoidal PWM technique, three modulating signals are compared with the triangular pulses to produce the pulses for active mode operation. To have shoot through mode, the positive and negative envelopes are compared with the triangular carrier signals. Whenever the triangular carrier signal is greater than the positive envelop or triangular carrier is lower than the negative envelop shoot through pulses are produced. This pulse is given to the switch S_0 to provide the boosting action. The shoot through pulses are inserted with the pulses of active mode and then given to the switches S_1 - S_6 .

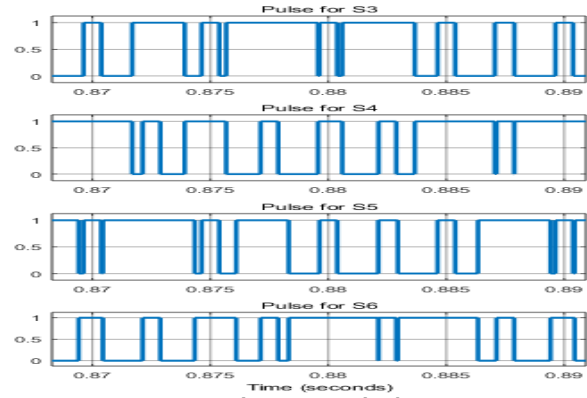
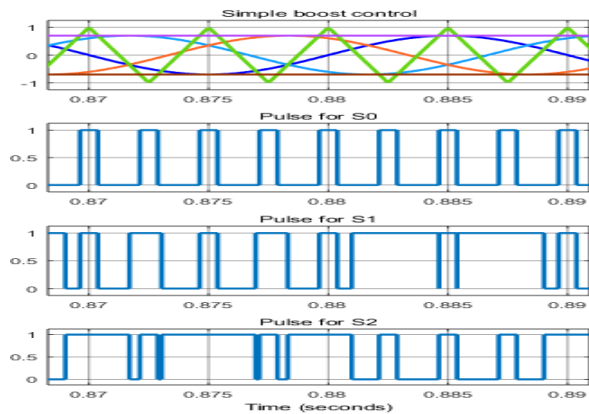


Fig.3 Simple Boost Control technique

A. Boost network components design[23]

The boost network has capacitors C_0 and C_1 , inductance L_1 . The ripple content in the inductor current is calculated as,

$$\Delta I_{L1} = \frac{V_{in} + V_{C0}}{L_1} DT \quad (19)$$

where T is the switching frequency of the inductor.

Current ripple in the inductor is given as,

$$r_L\% = \frac{\Delta I_{L1}}{I_{L1}} \quad (20)$$

The value of inductor L_1 is given as,

$$L_1 = \frac{D(1-2D)I_L R_i}{2r_L\%(1-D)} \quad (21)$$

Voltage ripple of the capacitor is given as,

$$\Delta V_{C1} = \frac{I_{L1} - I_{PN}}{C_1(1-D)T_L} \quad (22)$$

$$\Delta V_{C0} = \frac{I_{PN}}{C_0}(1-D)T_L \quad (23)$$

The capacitance values C_0 , C_1 are derived as,

$$C_1 = \frac{2(1-D)^2 T_L}{r_{C1}\%(1-2D)R_i} \quad (24)$$

$$C_0 = \frac{2(1-D)^2 T_L}{r_{C0}\%R_i} \quad (25)$$

where R_i is the load resistance.

IV. SIMULATION RESULTS

A 500W three phase SC based qSBI is designed. The MATLAB/SIMULINK based simulation is done to validate the performance of the inverter topology. The design parameters for the simulation are as follows: input voltage V_{in} = 100V, inductance L_1 is chosen as 5mH. The capacitances C_0 and C_1 are calculated as 1000 μ F and 1000 μ F. The star connected resistive load of 180 Ω /phase is considered. The shoot through duty ratio D is taken as 0.26 and modulation index M is considered as 0.7. The Switching frequency f_s is kept as 20kHz. While doing the simulation, on state resistance of the diode in the MOSFET is taken as 0.01 Ω and drain to source on state resistance is set as

0.1 Ω . The on state resistance of diodes D_1 , D_2 and D_3 is taken as 0.001 Ω , snubber resistance and capacitance are considered as 500 Ω , 250nF respectively. The simulated waveforms are shown as follows.

Fig. 4 shows the source voltage and source current waveform. It is understood from the figure that the source current of 4.99A is obtained with the source voltage of 100V. Fig.5 shows the voltage stress across the switch S_0 .

It is observed as 130V. The capacitors voltage V_{C0} and V_{C1} are obtained as 120V and 115V respectively as shown in Fig.6. Fig.7 shows the dc link voltage and dc link current waveforms. It is observed that the peak dc link voltage of about 235V.

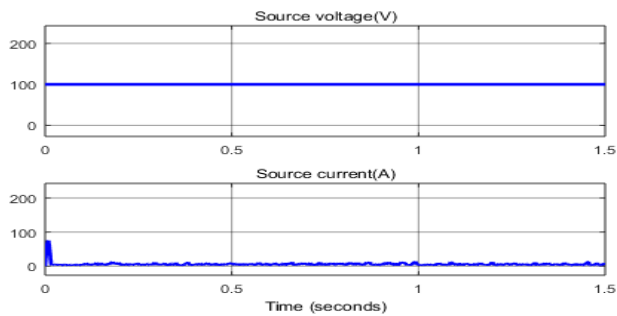


Fig.4 Source voltage and source current waveform

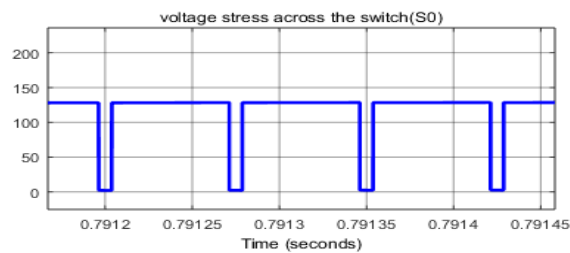


Fig.5 voltage stress across the switch S_0

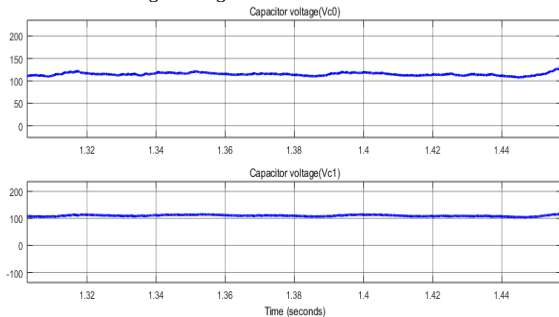


Fig.6 Capacitor voltage waveforms

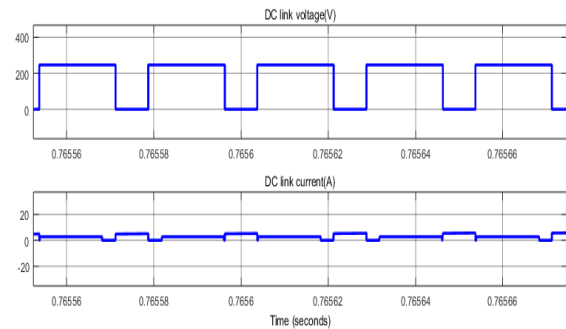


Fig.7 DC link voltage and DC link current waveforms

Fig.8 shows the unfiltered load current waveforms. The magnitude of load current is obtained as 2.2A at the inverter terminals. The Unfiltered load voltage waveforms are shown in Fig. 9. It is observed that the peak load voltage of 230V across the load.

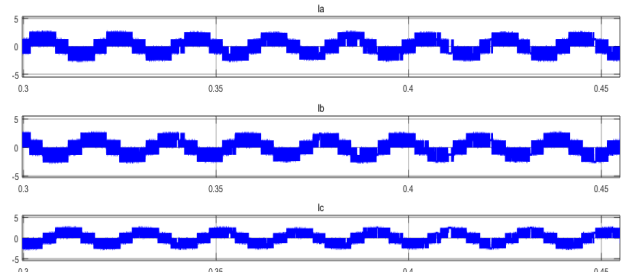


Fig.8 Unfiltered Load current waveforms

Fig.10 shows the filtered load voltage and load current waveforms. The filtered load voltage of 155V and load current of 2.2A are obtained.

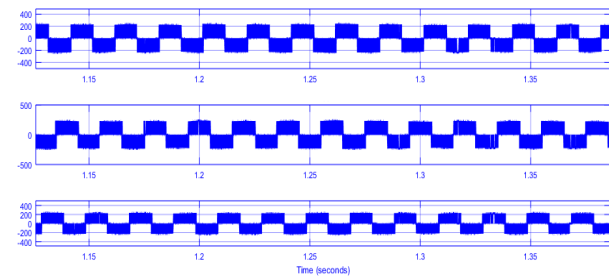


Fig.9 Unfiltered load voltage waveforms

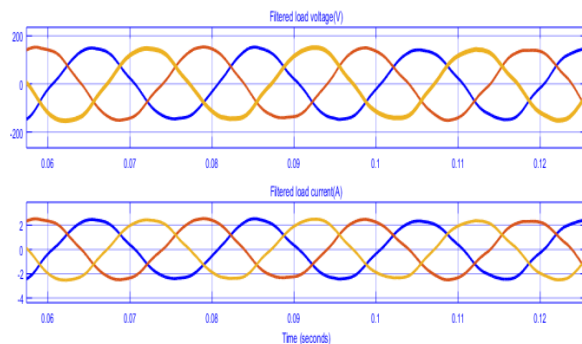


Fig.10 Filtered load voltage and load current waveforms

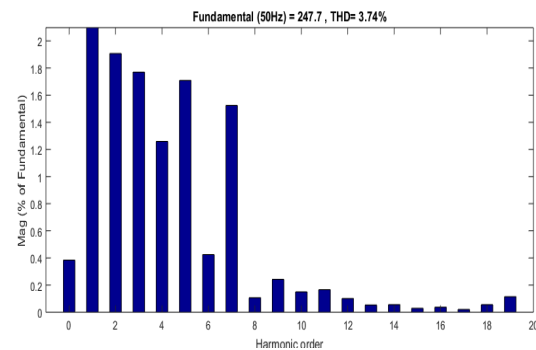


Fig.13 Harmonic profile

A. Performance analysis of three phase SC based qSBI

The proposed topology is designed for 110V (rms) per phase with the input voltage of 100V. The relation between boost factor (B) and the duty ratio (D) for various single stage boost inverter topologies are given in Fig.11. It is observed that the low value of duty ratio SC based qSBI can give higher boosted voltage and hence higher gain. Also the relationship between modulation index (M) and voltage gain (G) is shown in Fig.12. With the higher value of modulation index higher boost can be attained and the harmonic content in the load voltage is reduced. Fig.13 shows the harmonic profile of three phase SC based qSBI. It is observed as 3.74%. It meets the IEEE standard.

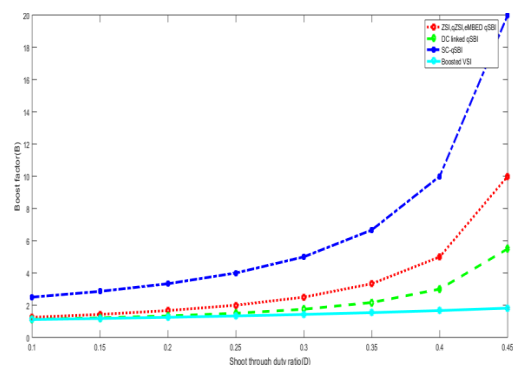


Fig.11 Shoot through duty ratio (D) Vs Boost factor(B)

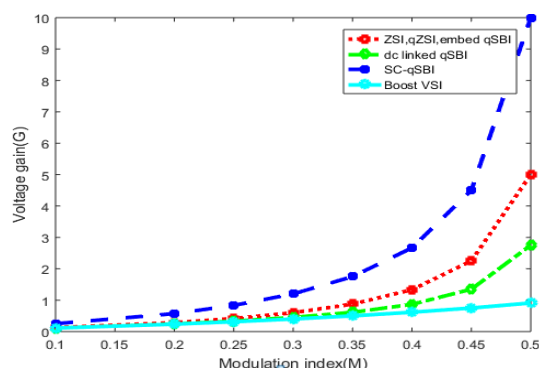


Fig.12 Modulation index (M) Vs Voltage gain (G)

B. Conclusion

In this work, a three phase switched capacitor based quasi switched boost inverter topology is discussed. With the input voltage of 100V, the peak ac voltage of 155V per phase is obtained with the THD of 3.74%. With the output power of 495W, the efficiency is calculated as 99% in simulation. There are some losses due to the on state resistance in the MOSFET switches and diodes as well as forward voltage drop across the diodes. So efficiency is reduced. In the hardware implementation, the optimal selection of devices can give higher efficiency. This research work can be further extended with the hardware implementation for PV applications.

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