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Design and Optimization of FINFET Based Schmitt Trigger Using Dual Sleep Method

Metikela Dhanalakshmi[1] metikeladhanalakshmi009@gmail.com[1]

Dr. D.R.Srinivas[2] srinivasgprec@gmail.com[2]

[1]PG Scholar, VLSI and Embedded Systems, G.PULLA REDDY ENGINEERING COLLEGE (AUTONOMOUS), KURNOOL, A.P.

[2]Associate Professor, Department of ECE, G.PULLA REDDY ENGINEERING COLLEGE (AUTONOMOUS), KURNOOL, A.P.

Abstract: In this paper, we designed Schmitt trigger using CMOS low power design technique at 180nm nm technology. With the advancement of technology, different parameters have been calculated Such as power-consumption, delay, power delay product (PDP), energy delay product (EDP) and noise. Different techniques are applied for the reduction in power consumption at the trade off with delay and area. In this paper we use novel FINFET based dual sleep technique is used to decrease the leakage power in the circuit. Schmitt trigger is a positive feedback amplifier that converts any continuous time varying signal to pulse wave. It forms the comparator of modern analog to digital convertor circuits, and it provides good noise immunity, thus it is used in communication. Parameters are calculated in both conventional CMOS based and FINFET based dual sleep technique and compared. The Average leakage power obtained using dual sleep method is 99.49PW which is very less as that of Conventional CMOS is 383.03uW Designing is done with variable voltage supply and the performance of the circuit is observed at different points. The circuit is simulated in Cadence virtuoso tool version 6.1 output of all is compared.

Keywords: CMOS, FINFET, Noise, leakage power, propagation delay.

I. INTRODUCTION

Schmitt trigger is an op-amp which works in positive feedback mode. The inverting terminal is connected to the reference input or ground. It converts any analog signal to digital pulse signal. By using op-amp gives rise to drawbacks like caused by large closed loop gain of op-amp, bigger area and limited value of resistors. Thus it is being designed using 6T CMOS. It is used for noise immunity with adjustable hysteresis width which we can attain using different techniques.[1] Some designing were done in 180 nm and the position of PMOS was changed to parallel from series connection to improve the delay in the circuit. [2] Different methods are being to designing of Schmitt trigger circuit and one of them is by current source and current sink. To get perfect output wave with respect to input. [3] It follows different gates, such as Schmitt inverter and using VTCMOS (variable threshold CMOS). When VTCMOS is applied in place of Schmitt inverter the performance gets enhanced and also with comparative energy-delay product.[4] Different techniques are applied to enhance circuit performance and hysteresis width and will improve the noise immunity in the circuit. The number of transistor for designing Schmitt trigger has changed from 6T for first stage and 4T for second stage. [5] With the decrease in number of transistors the supply voltage is also reducing and with better hysteresis width. [6] storage element's can be designed using Schmitt trigger. Designing of D latch is done with Schmitt trigger and pass transistor logic. This is used for the masking of small transition that occurs in any pulse.[7]Low energy-delay product, delay, will give us a better

circuit, so SBT (self biasing technique) are being used to reduce these parameters and to improve the output performance. [8] With the help of dual control gate floating gate transistor (DCGFGT) technique adjustable Schmitt trigger has been designed. This technique helps in the controlling the gate voltage in the circuit. [9] Hysteresis width can also be altered using design variation and thus noise immunity in circuit. [10] Schmitt trigger using FINFET is used for the reduction in leakage power at different supply voltages and compared. we have only one threshold level in comparators while in Schmitt trigger we have two different threshold voltage level (Vthh-Vthl) and thus known as trigger. It provides better noise immunity with the fact that it operates in threshold voltage level. Transition starts from zero and when it cross the upper threshold level then there is no change in output and we get a steady output unless it crosses the upper threshold level again and it's the same for negative threshold also. When noise is coupled to the signal during transition there is no change in the output as it gives a fixed pulse and thus it gives good immunity. There are various applications of Schmitt Trigger in both analog and digital domain. In the analog domain it is used for the designing of different circuits like OTA(Operational Transconductance Amplifier), CDTA (Common Differential Transconductance Amplifier), voltage controlled oscillator, level shifter etc. It is used as ADC for converting analog signal to digital signal. It is also used for designing different gates and memory cells

II. LITERATURE SURVEY

Low Power of FINFET Based Schmitt Trigger using Dual Sleep Method

This paper describes about the design and optimization of FINFET based Schmitt Trigger using Dual Sleep Method and it reduces power, delay and noise. This paper achieves low power and noise and high speed performance. CMOS Schmitt Trigger 6T offers high power of 383.03uW. To overcome above drawback we design an FINFET Schmitt Trigger and FINFET using Dual Sleep Method, it offers low power , propagation delay and noise parameters .

III. EXISTING SYSTEM

CMOS SCHMITT TRIGGER

Input of Schmitt trigger can be of any shape like sine wave, triangular wave, pulse wave etc. As shown in fig.3, when the input signal goes low PMOS I and PMOS2 will be ON and the output goes high, thus turning ON NMOS3. Since NMOS3 will be in saturation mode the output will be a constant high pulse signal and it will stay like this until next transition. When transition of input pulse goes from low to high then NMOS I and NMOS2 will be ON and the output will be low which will turns PMOS3 to ON state and the output we will be a constant low signal.

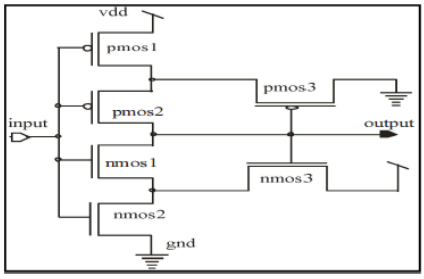

Fig .1 Conventional Schmitt trigger

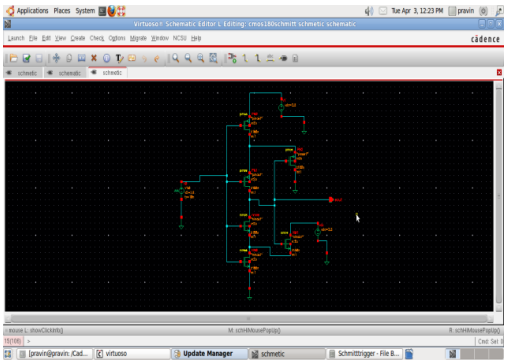

Fig 2. Conventional Schematic design of Schmitt trigger

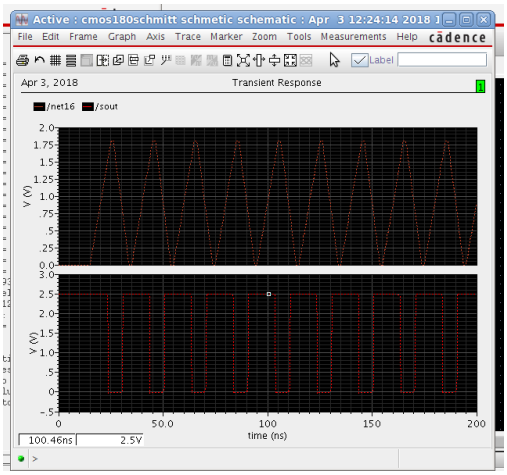

Fig.3. Transient Response of CMOS Schmitt trigger

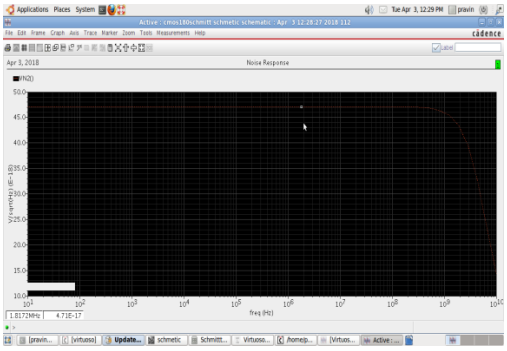

Fig.4. Noise response of CMOS Schmitt trigger

IV. PROPOSED SYSTEMS

Schmitt trigger is designed with FINFET technique as shown in fig 5. As an additional pin is attached to the transistor thus called as FINFET. It was developed by University of California for the reduction of leakage other short channel effects.

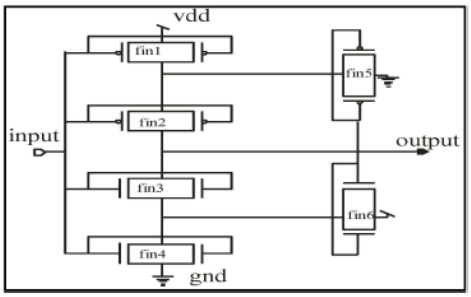

Fig 5: FINFET based schmitt trigger

The channel is placed above the body and gate is attached to it from three sides, so we get a good and controlled output from it. A better controlling of voltage can be achieved by using FINFET. A number of gates are joined together for better operation. The output resolution is better than conventional bulk CMOS design. Output obtained after the transistor sizing is much clear and with less distortion. The working of the proposed circuit is same as that of the CMOS with increased operating speed.

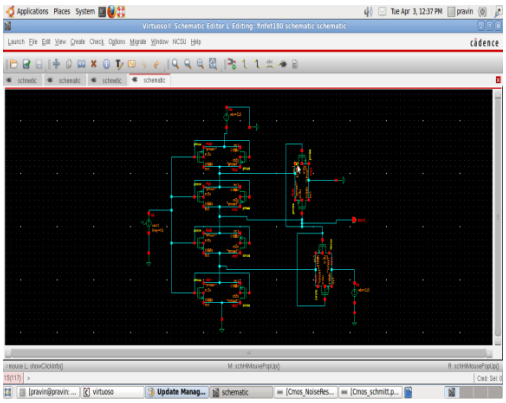

Fig.6.FINFET based Schmitt trigger

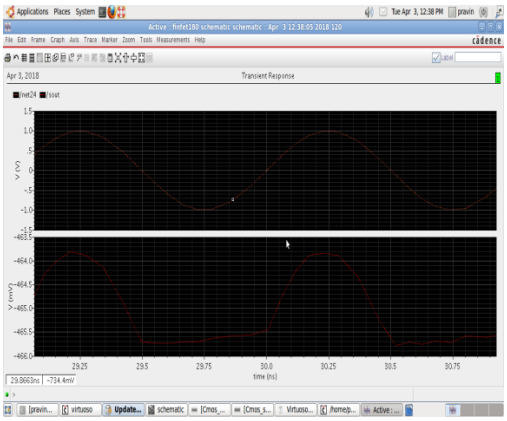

Fig.7. Transient response of FINFET based schmitt trigger

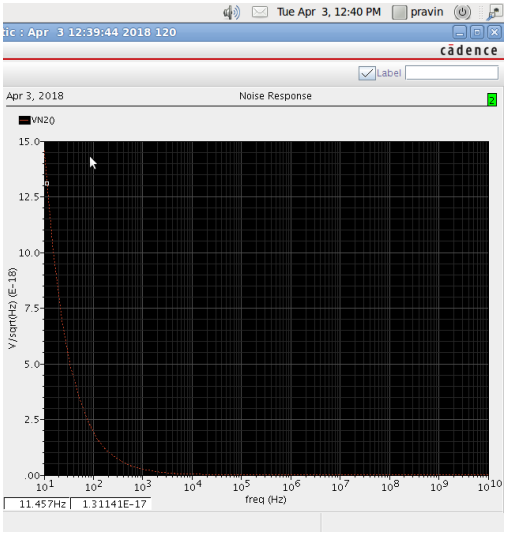

Fig.8. Noise response of FINFET based schmitt trigger

V. ENHANCED SYSTEM

FINFET USING DUAL SLEEP METHOD

SLEEP TRANSISTOR TECHNIQUE:

It proposes the use of sleep transistor for leakage reduction, which are also called gated -VDD and gated-GND techniques. This technique is used to cut-off both networks from supply voltage.

Schmitt trigger is designed with FINFET based dual sleep technique as shown in below schematic

Fig 9.Dual sleep technique design is more efficient in terms of power and delay compared with conventional CMOS and FINFET.

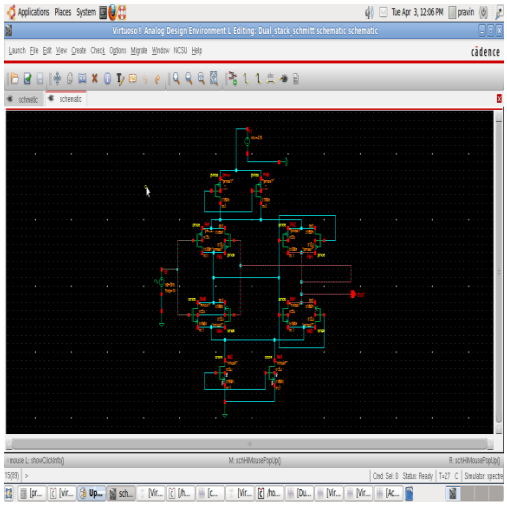

Fig.9. schematic of DUAL SLEEP TECHNIQUE

Dual sleep Technique uses the advantage of using the two extra pull-up & pull-down transistors in sleep mode either in OFF/ON state. To all logic circuitry the dual sleep portion is designed as common. For a certain logic circuit less number of transistors are enough to apply.

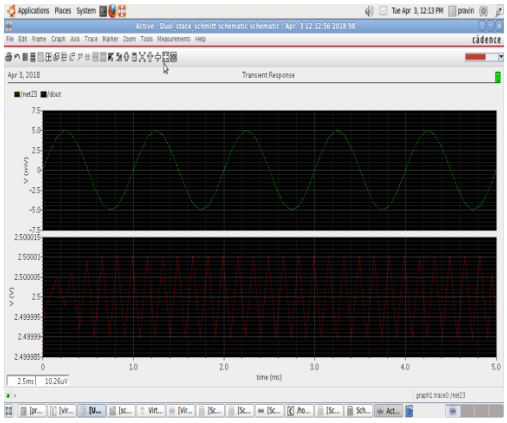

Fig.10. Transient response of DUAL SLEEP TECHNIQUE

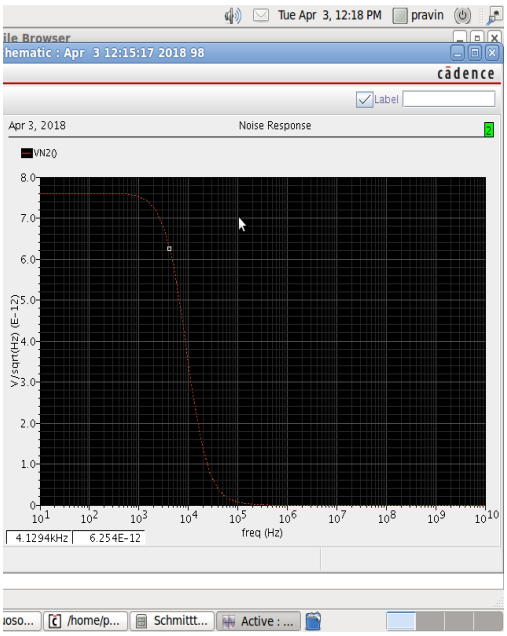

Fig.11. Noise response of DUAL SLEEP TECHNIQUE

VI. PARAMETER ANALYSIS OF DESIGNED CIRCUITS

a) Noise:

Noise in any circuit causes fluctuation of the supply voltage that distorts the signal frequency which affects the output of electronic circuits.

Sv(f) = 4KTR, f>=0 -----→(1)

Where K=>Boltzman constant.

T=>temparature.

R=>Resistor.

b)Power Consumption:

It is defined as the leakage current ICC(current into a device) along with the supply voltage (VDD).

Power (P) = (Vdd) * (Iavg) (2) V dd is the supply .

CMOS = 386.6uW.

FINFET = 10.05PW.

Dual sleep = 99.65PW.

c)Propagation Delay:

Delay refers to time lag between departure of the signal from source and the arrival of the signal at destination. It is less in dual sleep technique compared with existing and proposed system.

Delay of CMOS = 1.924ns

Delay of FINFET = 10.1Ps.

Delay of Dual sleep =660.5Ps

d) Energy delay product:

It is the product of power consumption (averaged over a switching event) times the input-output delay, or duration of the switching event.

$$EDP = P_{avg} * t_p$$

Where P_{avg} is the average power

t_p is the propagation delay

CMOS: 7.42664×10^{-12}

FINFET: 1.242136×10^{-20}

DUAL SLEEP: $6.5713145 \times 10^{-20}$

VII DESIGN SUMMARY

PARAMETERS	CMOS	FINFET	DUAL SLEEP
1)POWER CONSUMPTION	386.6uW	10.05PW	99.65PW
2)PROPAGATION DELAY	1.924ns	10.1Ps	660.5Ps
3)ENERGY DELAY PRODUCT	7.42664×10^{-12}	1.24213×10^{-20}	$6.5713145 \times 10^{-20}$
4) NOISE	4.71×10^{-17}	1.31141×10^{-17}	6.254×10^{-12}

VIII CONCLUSION

This paper is designed in 180nm technology using CMOS, FINFET and FINFET based dual sleep technique. Bulk device consumes more power and the resolution of the output is also not proper. The simulation of the proposed circuit is done with supply voltage of 1.8 V and with the frequency of 100M Hz where we obtain a better output performance. By using FINFET and dual sleep technique there is reduction in the power consumption and propagation delay. Finally We conclude that using the FINFET technique and dual sleep technique it improves the circuit performance in terms of Power, delay, noise and energy delay product.

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