

IMPROVING POWER QUALITY IN SOLAR FED CASCADED MULTILEVEL INVERTER WITH MINIMUM NUMBER OF SWITCHES

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Abstract - In this project, Cascaded Multilevel Inverters (CMLIs) are used which has the advantages that it eliminates DC-DC boost converter and voltage unbalance problems. Modified Multilevel Connection is designed to decrease the number of switches in the standalone/grid interacted solar photovoltaic (PV) systems. In conventional method to obtain 15 level inverter, 28 switches were used. In binary and trinary modes, it is reduced to 12 switches to obtain 15level inverter. In proposed system, by using Modified Multilevel Connection (MMC), the number of switches is reduced to 7 to attain 15level inverter. Total harmonic distortion (THD) is reduced by increasing the levels which in turn reduces the usage of number of capacitors and diodes.

KEYWORDS

Cascaded multilevel inverter, MMC, Photovoltaic, Total Harmonic Distortion

I. INTRODUCTION

We mostly use conventional sources for the production of electrical energy. This makes increased greenhouse gas emissions and other societal issues. Nowadays, solar energy is the emerging renewable energy sources. Sunlight falling on the solar panel is converted into electrical power. This electrical power is saved on the battery as dc source. It is converted to ac by using the inverter for ac loads. This inverter plays a vital role in the solar energy production. For solar power plant we use multilevel inverter for getting output in various levels.

Harmonic content is reduced in the voltage and current waveforms by the multilevel inverter. By using multiple connections we can get different levels of output. Harmonics is multiple of the fundamental

frequency. Power quality problems in the grid are mainly due to harmonic frequencies. Harmonics usually occurs in current and voltage wave forms, which repeat at every cycle. Harmonic distortion is decreased by increasing the number of levels. Cascaded Multilevel inverter is preferred for renewable energy system due to the absence of voltage unbalance problem, clamping capacitors, diodes, removal of DC-DC boost converters.

This paper is organised as follows: Section 2 explains the existing system, Section 3 explains the proposed system, Section 4 explains the switching strategy of the proposed system, Section 5 explains the simulation and results, Section 6 explains the experimental results and Section 7 explains the final conclusion of the paper.

II. EXISTING SYSTEM

In the existing system, by using 12 switches, 15 levels output is obtained. Pulse width modulation (PWM) techniques are used in conventional approach. The required gate pulse for the inverter switches is provided by matching the reference and carrier signals. The following equation gives the number of output voltage levels,

$$m = 2N_s + 1$$

Where, m - output voltage level

N_s - Number of inverter stages

For m - levels, the number of switches is calculated by the following equation,

$$l = 2(m-1)$$

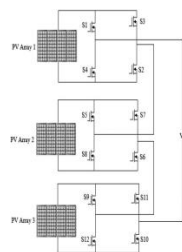


Fig 1. Three Stages Cascaded Multilevel Inverter

For 15 levels CMLI, 28 switches with seven individual inverter stages are required, 182 clamping diodes are required for neutral point clamping (NPC) method. 91 balancing capacitors and 14 DC bus capacitors are required to achieve 15 levels output in case of FC type multilevel inverter. In Fig 1 the three stages cascaded multilevel inverter is shown using 12 switches to achieve 15 - levels.

III. PROPOSED SYSTEM

In proposed system, a digital logic control circuit is proposed without the use of bidirectional switches to

achieve higher levels. Transformers, filter components, detailed look-up table are not necessary. Here 15-level is achieved by 'Modified Multilevel connection'. In conventional method, Pulse Width Modulation (PWM) technique is used. But using PWM technique, transformer and ultra-capacitors the overall cost will be more. Manufacturing inverter using the above mentioned elements can cause difficulties and it is not desirable for the application of motors. In MMC, a single stage inverter is used to achieve 15-level. In this method, input voltages are added by using embedded controller. Based on the suggested switching sequence, the embedded controller will work. In both the control and power circuits modifications are made to obtain 15 levels with only 7 switches. By using Modified Multilevel Connection approach, using of 7 switches is achieved. The diode and capacitor (1nF) are added in the existing circuit to normalise the output. The required output voltage is obtained by turning on T - T4 at all stages by controlling S1 - S3. The input voltage is controlled to achieve 15 levels by operating the ON/OFF status. The rest of levels in the truth table are deduced by reversing the sequence.

We get the inputs V1, V2, V3 from the PV array. When V1 gets the input, V2 and V3 are in OFF state. By controlling the ON/OFF states, 15 levels is achieved. Using the proposed switching sequence it can be controlled in reverse direction.

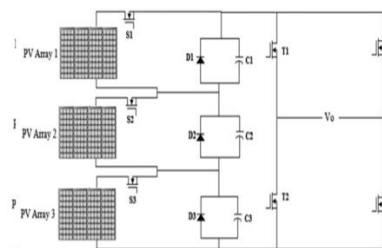


Fig 2. Single stage 15-level inverter power circuit

IV. SWITCHING STRATEGIES

Level	S1	S2	S3	T1	T2	T3	T4	V _o
0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	1	48
2	0	1	0	1	0	0	1	96
3	1	1	0	1	0	0	1	144
4	0	0	1	1	0	0	1	192
5	1	0	1	1	0	0	1	240
6	0	1	1	1	0	0	1	288
7	1	1	1	1	0	0	1	336

Table1. Switching sequence of 15-level inverter with MMC

ON and OFF conditions of the inverter circuit (T1-T4) for all the levels is shown in the above table. But the required output voltage is obtained by controlling the input switches (S1-S3).

Let V1-V3 be the inputs of PV array. During 1st level, only V1 is given as input to the inverter circuit and V2, V3 in OFF condition. Similarly controlling the ON/OFF status of the input stages, 15 levels is achieved. If the sequence is controlled in reverse direction, the remaining 7 level will be obtained.

V. SIMULATION AND RESULTS

The embedded-based controller provides the gating signals in addition of input voltage, based on the switching sequence. The voltage inputs are given in three different levels as 48, 96 and 192 V. By reducing THD, the power quality is considerably increased. Simulation is done for both the existing and the proposed system and the results are compared. The full circuit is implemented with the solar PV panel input. The inverter output frequency is 50Hz. In the simulation circuit, filter is added to reduce the Total Harmonic Distortion to a greater extend. Simulation is done for both the circuits with and without filter and the comparison is analysed

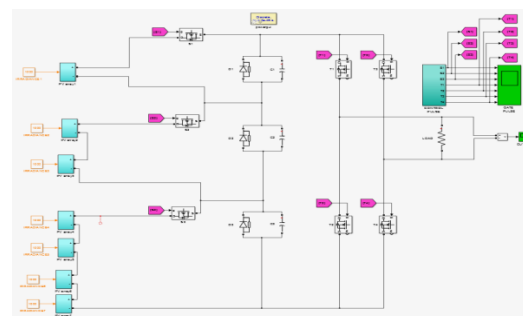


Fig 3. Digital switching circuit for 15-level CMLI without filter

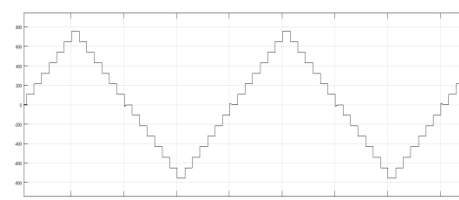


Fig.3.1. 15- level output voltage waveform without filter

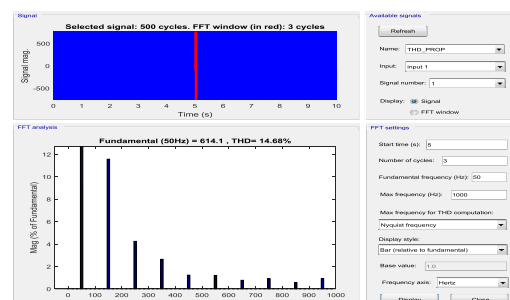


Fig.3.2. FFT analysis for three stage 15-level CMLI without filter

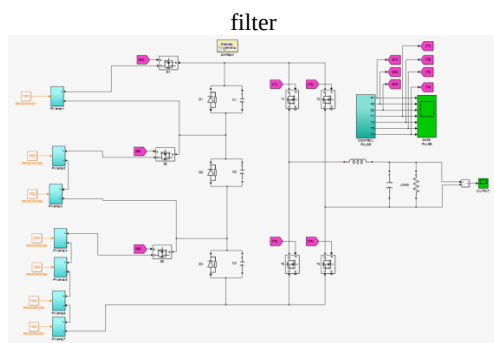


Fig 3.3.Digital switching circuit for 15-level CMLI with filter

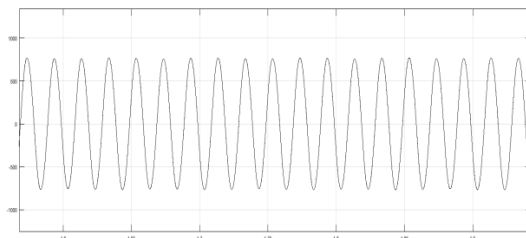


Fig 3.4.15-level output voltage waveform with filter

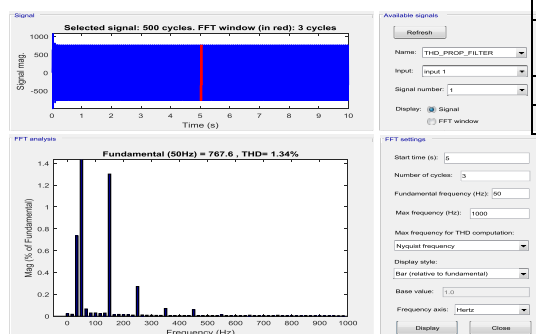


Fig 3.5.FFT analysis for three stage 15-level CMLI with filterIn Fig 3 the simulations design circuit of 15-

level CMLI without filter is shown. In this (fig 3) circuit 12 switches are reduced to 7 switches by Modified Multilevel Connection (MMC).

In Fig 3.1 output voltage waveform of 15-level CMLI without filter is shown. The output is in the step waveform.

In Fig 3.2 the FFT analysis for three stage 15-level CMLI without filter is shown. The Total Harmonic Distortion (THD) of the 15-level CMLI without filter has the value of about 14.88%.

In Fig 3.3 simulation design circuit of 15-level CMLI with filter is shown.

In Fig 3.4 the output voltage waveform of 15-level CMLI with filter is shown. The output is in the sine waveform.

In Fig 3.5 the FFT analysis for three stages 15-level CMLI with filter is shown. The Total Harmonic Distortion of the 15-level CMLI with filter has the value of about 1.34%.

VI. COMPARISON OF EXISTING AND PROPOSED SYSTEM

S.NO	SYSTEM	THD VALUE
1.	EXISTING WITHOUT FILTER	20.78%
2	PROPOSED WITHOUT FILTER	14.68%
3	EXISTING WITH FILTER	1.96%
4	PROPOSED WITH FILTER	1.34%

VII. EXPERIMENTAL RESULTS

The proposed method is implemented and analyses were made. The entire hardware specifications are listed in the table 2. The hardware setup has three major circuits control circuit, driver circuit and the main circuit.

A. CONTROL CIRCUIT

Pulses are generated for switches in the main circuit with the help of PIC controller.

The pulse from the control circuit gives the signal into the Driver which is used for amplification and isolation purpose.



Fig.7.1 Control circuit

The control circuit has crystal oscillator KDS10.000. The input is first rectified by using the bridge rectifier (DZW10). The rectified input is regulated by using the voltage regulator (IC7805). The capacitor used here has the value of $100\mu\text{F}$, $470\mu\text{F}$, $0.1\mu\text{F}$. The control circuit has PIC microcontroller (PIC16f877a). The output from the voltage regulator is given to the PIC microcontroller. The output of the control circuit is given to the driver circuit.

B. DRIVER CIRCUIT

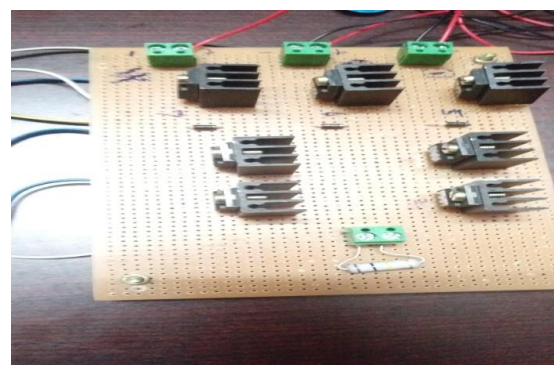


Fig 7.2 Driver Circuit

The driver circuit generates necessary pulses for the switches in the main circuit. The driver circuit has the Optocoupler (TLP250). The optocoupler is used to transfer electrical signals between two isolated circuits. Snubber circuit is used to prevent the back flow of charges to the supply. During supply the diode in the snubber circuit is forward biased and it will become reverse biased during the back flow. The value of capacitor and diode used in the driver circuit $470\mu\text{F}$ and IN4001. Resistor is used to prevent the high currents. The values of resistor are $15\text{k}\Omega$, 400Ω , 100Ω .

C. MAIN CIRCUIT

The proposed Modified Multilevel Connection is implemented on the main circuit. The main circuit has 7 switches. The switching actions of three switches in the input side is monitored and controlled. The switches S1-S3 can be turned on as per the sequence to further add the input voltage. The full bridge inverter circuit is formed by the switches T1-T4. By using Modified Multilevel Connection, 15-level output is achieved by using only 7 switches. Hence, the number of switches used and the harmonic distortion are reduced.



The prototype of the hardware is implemented where the input given is in the range of 9, 18 and 27V. The harmonic distortion value reduced is same for this value of inputs. For higher value of inputs we can use battery of high voltage value. The main advantage of the proposed method is the absence of transformer

HARDWARE SPECIFICATIONS

CONTROLLER CIRCUIT

PIC Controller	: PIC16f877a
Voltage Regulator	: IC7805
Capacitor	: 100 μ F, 470 μ F, 0.1 μ F
Battery	: 9V
No of batteries	: 7

VIII. CONCLUSION

By reducing the number of power electronic switches and the number of levels, power quality improvement is made and the Total Harmonic Distortion is reduced. In MMC mode, using 7 switches 15 level output is

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Crystal Oscillator	: KDS10.000
Resistor	: 900 Ω , 400 Ω
Bridge Rectifier	: DZW10

DRIVER CIRCUIT

Optocoupler	: TLP250
Capacitor	: 470 μ F
Diode	: IN4001
Resistor	: 15k Ω , 400 Ω , 100 Ω

MAIN CIRCUIT

Switch	: MOSFET IRF840
No of switches	: 7

achieved. We have done both the simulation and hardware implementation and successfully obtained the desired output. The following advantages like reduced THD, Simple design, less cost, minimum computational complexity are observed.

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