Comparative Analysis and Design of Full Adder using Domino Logic and Various Logic Styles

Harini.V1, P. Sasi Searthi2, G. Vishnu Vardhan Rao3
1,2 U.G. Student, 3 Assistant professor
1,2,3 Department of Electronics and Communication Engineering
1,2,3 Vel Tech Multi Tech Dr. Rangarajan Dr. Sakunthala Engineering College
Avadi, Chennai – 600062

Abstract— With the demands of upcoming technologies, furthermore the difficulties of nano meter-era of VLSI designs and logics require new advanced logic strategies and methods that are in the meantime elite, better performance, energy efficient and robust and noise immune. Dynamic CMOS circuits are comprehensively employed to plan high end networks that result in better performance, because of their speed. Then again, the key negative mark of dynamic logic style is its more vulnerability to noise. The principle case behind this is the sub-threshold leakage current coursing across the NMOs branch of the designed system. With persistent innovation scaling, this issue is getting increasingly serious. In this project, another noise immune dynamic CMOS circuit method is suggested. The suggested method provides better power and delay. In this paper portrays the less power, noise immune and speedy domino logic method. Simulation results demonstrated using CMOS technology of 180 nm when we utilize proposed method for recognizing large fan-in logic circuits, so that it can attain peak value of noise robustness as contrast with the fundamental component.

General Terms - Full Adder, CMOS, VLSI

Keywords—power delay product(PDP), Static CMOS, Pseudo NMOS, Domino logic, Proposed Domino logic.

1. INTRODUCTION

In modern technologies, the systems focus on smaller area size, lesser cost of expense and faster computation time. These demands have been met using VLSI technology that allows an increase in the operating frequency while facilitating lower delay. Research scholars have analyzed that the design strategy and amount of power dissipated and consumed must always be taken into consideration at various level of design.

Parameters like execution of the circuit, power and strength are specifically influenced by the type of logic style decided for the circuit. CMOS circuit outlines are significantly sorted into static and dynamic logic in spite of the fact that do not match the demands of the future working systems. Static CMOS rationale is straightforward, simple and vitality effective however it possesses large area and require 2N transistors which make it hard to be utilized as a part of vital circuits. Domino logic is speedier, occupies lesser area yet devours more power when contrasted with static circuits. Therefore, an enhanced digital logic method has similar time energy proficient, speedy and noise robust is essential.

In this paper, footed logic circuit is implemented by semi-domino logic for has been suggested. Using this method, unnecessary signals of the dynamic node, this signals produced in the precharge operation, this signals will be blocked before reaching the output point, for the traditional instance. As a consequence, a more power is stored as contrast to different domino logics. This circuit will get a improved energy-efficient, robust and more-speed will be achieved in this method by utilizing footer and keeper transistors.
Same circuit is designed with different methods and is peer analyzed and compared. To demonstrate advantages of the proposed logic is designed with cadence virtuoso 180 nm software tools.

II. LOGIC STYLE

Speed, power dissipation, size and wiring complexity are affected by Logic style of a circuit. Circuit delay will be decided by wiring capacitances, transistor sizes and Number of transistors in series.

1. Static CMOS method

VDD or GND will be attached each gate output is via less resistance track in static technique. Static CMOS design consists of a pull up network (PUN) which is connected to VDD in this we will use PMOS transistors and where as in a pull-down system (PDN) connected to GND in this we will use NMOS transistors as portrayed in Fig. For an occasion one of the PUN or PDN block is on; with the goal that either at VDD or GND will remains at the out node. The PUN and the PDN are mutually exclusive of each other, meaning only one of them is ON at a particular instant.

![Fig 1: Static CMOS inverter](image)

2. Pseudo NMOS Logic

2.1 Ratioed Logic

The ratioed logic has pull down networks made of NMOS transistors and pull up networks which could be resistors, PMOS or NMOS. Each of these configurations of PMOS exhibits different characteristics output. The fig 2 shows resistive load. This configuration is unsuitable for low power design VLSI design as it requires large space requirement of resistor in a silicon substrate. Let us assume that the resistance of both pull up and pull down are linear. In that case the noise margin is low.

In order to keep up the noise margin the resistance should be as follows

\[ R_L >> R_D \]

Where,

\[ R_D \] – pull down network resistance
\[ R_L \] – load resistance

To achieve this, we need to increase the ratio as follows

\[ (W/L)_D / (W/L)_L > 4 \]

![Fig 2: Resistive load](image)

2.2 Pseudo NMOS technique

another type of ratioed logic is Pseudo NMOS technique which has pull up network only one PMOS transistor. The gate of the PMOS transistor is joined grounded permanently. The PMOS is 5 times weaker than NMOS. The following figure shows basic pseudo inverter circuit. Here \( Q_P \) is the pull up
PMOS transistor which acts as load. The transfer characteristics of depletion mode pull up and PMOS pull up are same. Therefore, it is called pseudo NMOS logic.

![Fig 3: Pseudo NMOS inverter](image)  

The main advantage of this technique for an N-input logic function it require of N + 1 transistors. Whereas in CMOS logic it 2N transistors.

3. Domino Logic

Cascading problem in dynamic circuits can be eliminated in domino logic organization. It consists of dynamic logic and a static CMOS inverter. In precharge stage (CLK = 0), VDD will be connected to the output. So zero ill be the output of an inverter. OUT will be modify from zero to one in the evaluation stage (CLK = 1).

![Fig 4: Domino circuit](image)  

Once CLK goes zero, inverter buffer output is low because dynamic point is precharged to one. PDN network output change to zero. When CLK goes high, dynamic node discharged and the inverter output becomes one.

4. Proposed Domino Logic

A different method for domino logic has been proposed that can suppress the noise spikes and monotonicity of dynamic logic. This results in increased speed and decreased power dissipation in contrast to other existing domino logics. When compared with the static CMOS logic gates, noise sensitivity of domino gates is greater since of its low switching threshold voltage. For designing high fan-in gates those gates are noise immune has turn out to be a huge worry. Due to large number of transistors and complex network, because of sub-threshold leakage currents. Improved domino logic has been proposed to overcome the problem of noise intolerance, delay and power dissipation in domino logic circuits.
The suggested domino logic is illustrated in above fig 5. $M_3$ Transistor is utilized as a stacking transistor. For NMOS transistor in the PDN Gate source voltage decreases (stacking effect) due to voltage drop across $M_3$. The suggested logic will use an extra evaluation transistor $M_4$ In that CLK is connected to the gate terminal. When $M_1$ having a less voltage because of noise-signals, $M_2$ begins leaking of large power dissipation. Due to this circuit is a smaller noise robust. The transistor $M_4$ in the suggested scheme is the reason for stacking effect. So the gate-source voltage $V_{GS}$ of $M_2$ lesser ($M_3$ less conducting). So the circuit develops into less leakage power consuming.

### III. FULL ADDER USING VARIOUS LOGICS

The above-mentioned logics can be used to implement arithmetic circuits such as full adder, comparator etc. These are the basic circuits used in wide arithmetic applications. Decreasing the no. Of transistor will gives rise to lesser power consumption and great speed.

The full adder implementation using static, Pseudo NMOS, Domino and proposed domino circuits are given below.

1. **Static CMOS**

   The fig 6 shows the implementation of a 1-bit full adder using static CMOS which consists of 28 transistors.

   **Pseudo NMOS Logic**

   It consists of 18 transistors to implement sum and carry logic.
1. **Domino Logic**
The domino logic consists of 20 transistors used to implement sum and carry of full adder.

2. **Proposed Domino Logic**
It consists of 26 transistors to implement sum and carry logic.

**IV. RESULTS AND SIMULATIONS**
The depicted simulated waveforms of proposed and existing circuits were simulated at 1.8 Volt at 27°C using cadence spectre. The waveforms are the transient response of the circuits. The output conforms to the truth table of the full adder. For evaluation under similar environmental state, all these circuits have been simulated.
Fig 10: Simulation of Static CMOS FA

Fig 11: Simulation of Pseudo NMOS FA
V. TABULATIONS

<table>
<thead>
<tr>
<th>S. No</th>
<th>FULL ADDER</th>
<th>NO. OF TRANSISTORS</th>
<th>DELAY</th>
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<tbody>
<tr>
<td>1</td>
<td>Static CMOS</td>
<td>28</td>
<td>31.27E-9</td>
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<tr>
<td>2</td>
<td>Pseudo NMOS</td>
<td>18</td>
<td>19.14E-9</td>
</tr>
<tr>
<td>3</td>
<td>Domino logic</td>
<td>20</td>
<td>11.27E-9</td>
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<tr>
<td>4</td>
<td>Proposed domino logic</td>
<td>26</td>
<td>7.78E-9</td>
</tr>
</tbody>
</table>

Table 1: comparison of power, delay and PDP
VI. CONCLUSION
Using the proposed full adder a comparator is implemented. All the schematics were simulated under similar environmental state as that of proposed logic with same parameters. The earlier logics and proposed full adder was contrasted with the simulation results. It can be concluded that the proposed full adder has less delay and power delay product. The proposed domino full adder has 2.3 times less PDP than existing domino logic. The proposed full adder is 1.44 times speeder than the existing full adder.

VII. FUTURE SCOPE
The domino full adder can be used to design several logic functions which could be extended further to design an ALU. Additional noise deduction methods can be explored which would improve the performance. The schematics could be designed into a layout and further fabricated to real chip for several purposes.

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IX. REFERENCES


