

DESIGN OF CMOS CURRENT REUSE LOW NOISE AMPLIFIER USING MODIFIED ACTIVE INDUCTOR

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Abstract--A low power Low Noise Amplifier (LNA) is proposed using 180nm CMOS technology for the frequency of 2.6GHz. LNA is designed using current reuse structure where two transistors share same amount of current. Active inductor is used to replace the passive inductor using modified Gyrator-C topology. The modified Gyrator-C topology consists of two transconductance stages realized by common-source configuration with multi-regulated cascade stages. Active inductor causes significant reduction in chip area as compared to the passive ones.

The proposed LNA is simulated using cadence virtuoso in 180nm technology. The LNA has a flat gain at 2.6GHz frequency. The gain obtained by the LNA is about 17.32dB, noise figure is about 2.62dB. The proposed design gives an input return loss less than -17.7823dB and the power consumption is about 5.856mW.

KEYWORDS— Active Inductor, LNA, CMOS

I. Introduction

The implementation of advanced silicon Radio Frequency (RF) Integrated Circuits (ICs) is an

attractive option for the constant development of new device designs to meet the demand of wireless systems. Among these RF ICs, the use of CMOS technology has been shown to be trend. When observing the stages of an RF IC, the first block of the receiver is usually composed of the low noise amplifier - LNA (Low Noise Amplifier). Its low intrinsic noise and good gain have fundamental roles on all reception system noise. In the literature, it is verified that the common source and common port configurations of the CMOS LNAs have the same properties and limitations of the common emitter and common base configurations of the bipolar amplifiers. One exception is that for typical RF polarization dimensions and currents, CMOS devices are more linear than bipolar. . And among these configurations, the common port ends up being deprecated due to its greater intrinsic noise than the common source (typically 2-3 dB). During the development phase of an LNA design, the input impedance can be matched (usually at 50Ω) using some distinct topologies, such as parallel input

resistance, feedback resistance, inductive degeneracy, among others. The use of resistances resulting in increased noise. On the other hand, inductive degeneration using Passive Inductors (IPs) has the disadvantage of occupying a very large area in the IC, besides dependence on the quality factor (Q) of the inductors, which normally do not have satisfactory values. Despite the listed disadvantages, the inductive degeneration by PIs, since it does not add significant increase in noise, is the natural choice by most of the area's designers. Such degeneration can be accomplished by the use of IPs or by the wire bond itself of the CI / board interconnect. This is possible because typical values for such inductors are in the order of 1 to 2 nH, which can be implemented via wire bonds (around 0.7 nH / mm). However, the drain IPs, because they have higher values of inductance, is normally outside the reachable range through wire bonds. As their values are function of the operating frequency, it becomes possible to combine a proper tuning to a good impedance matching at the output. Thus, integrated IPs are usually found at this point in the circuit. As a consequence, alternatives to overcome such disadvantages have been proposed over time. Integrated Active Inductors (IAs) have been presented in the literature through circuits that emulate the effect of conventional IPs, based on the inductive behavior of the gyrator circuit. These circuits present a smaller dimension, possibility of adjustments of the inductance value, frequency of operation, and Q, to the cost of power consumption and a relative increase in total system noise. Several papers have been presented in the literature exploring the use of IAs in different applications such as:

amplifiers, oscillators and filters. The IAs are used in the LNAs fundamentally to couple the input or output impedances and as active load. Thus, a common source LNA using IAs may suppress the aforementioned problems. In this context it is proposed the design and analysis of an LNA cascode common source with use of IA in the Compact Wu Folded configuration (IA-CWF) and degeneration by wire bond (LNAIAWB) to operate in the 1.8 GHz band, aiming at possible applications in GSM / GPRS / EGPRS.

The development, design and application of the IA, which will be used as load inducer of the LNA, aims to decrease the amount of IP used and with that, optimize the total area occupied by the IC, thus reducing the size of its layout. Circuit modeling and analysis of simulation results, including edge and post-layout analysis, will evaluate the performance and feasibility of the proposed topology. For this, this article is divided into four sections besides this introductory section. In the second section the detailed LNAIAWB project is presented. The third section describes the main results obtained from the proposal, while in the fourth section the layout, as well as the post-layout analysis, is presented. Finally, the fifth section concludes the paper

II. Literature survey

This work presents a topology proposal of a 350nm CMOS cascode low noise amplifier using an active inductor in Compact Wu Folded configuration. Compact Wu folded configuration is the current reuse concept used in the active inductor. E. V. V. Cambero

et al., gave a novel method of replacing the passive inductor with the active inductor, optimizing the integrated area and power consumption and thus growing less the total dimension of the layout. With the advancement in the technology it is seen that 180nm technology is better than 350nm technology which can further reduce the integrated chip area.

III. Proposed system

Low noise amplifier (LNA) is a first crucial component in RF receiver design. The important role of LNA is to amplify the received signal with less noise. The linearity of LNA is improved by various linearization techniques such as feed forward, post-distortion, derivative superposition (DS) and modified derivativesuperposition. The expanding prevalence and development of wireless communication has increased research in the field of RFIC. The tremendous improvement in the performance of MOSFETs has enabled the RF applications. The main drawback which is noticed in this case is the large gate inductance (L_g).

Passive inductors are off-chip discrete parts and this seriously confines the bandwidth, diminish dependability, and expand the expense of framework. At that point creator's endeavors have obliged on manufacturing inductors on silicon mass keeping in mind the end goal to incorporate them by CMOS innovation. Meanwhile, the need for a large silicon area to fabricate spiral inductors has also sparked a great interest in and an intensive research on the synthesis of inductors and transformers using active devices, aiming at minimizing the silicon

consumption subsequently the manufacturing cost and improving the performance.

A. Current Reused LNA

The current reuse topology may provide the best combination of high power gain, low noise figure, and low power consumption, making it a feasible option for use in UWB LNA designs. In an amplifier employing current-reuse techniques, the input RF signal is amplified by two cascaded common-source amplifier stages to provide high gain. Simultaneously, this topology also supports low noise figures. The input matching circuitry is aided with the help of a high-pass filter to suppress noise. The basic issue with using CMOS transistor for LNA is its inherently low transconductance and hence low gain. However, if current reuse method is used, transconductance would be increased. The key point is that given the same bias current the effective transconductance is $g_{m1} \times g_{m2}$, while it is simply g_m in other cases. Single source results in less power dissipation. The current-reuse model can be considered as a two stage cascode amplifier, in which the first stage is the CS amplifier and the second stage is the cascode amplifier with an additional buffer stage at output end. The current reuse technique is well known for its use in LNAs, for its capability of achieving high performance with power consumption that is less than conventional two-stage common-source amplifiers. The fig. 4.1 shows a current reused LNA.

The proposed LNA is being described. Since, transistors M_1 and M_2 are connected in current reuse structure, M_1 and M_2 share the same bias current from the supply voltage. The current reuse LNA

supports high gain and low power consumption. The capacitor C_d is used to reduce gate induced noise. The ac signal is amplified by the main transistor M_1 and is coupled to the gate of common source stage M_2 by the capacitor C_2 . This two stage configuration increases the gain. The LNA is biased in strong inversion region. C_1 , L_g and L_s are the input matching network components. L_d and C_4 are the output matching network components. C_1 and C_4 are the DC blocking capacitors. C_3 is used to ground the ac signal. Inductor L_m is used to provide high impedance between two stages.

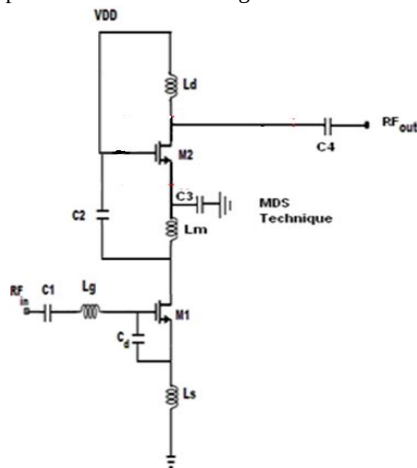


Fig. 1 Schematic of current re-used LNA

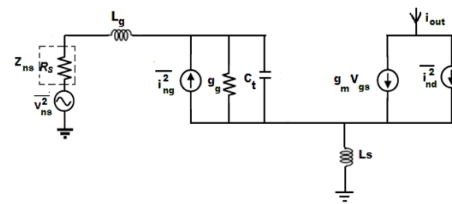


Fig 2 Small Signal Equivalent Circuit of input stage

The small signal equivalent circuit of input stage is shown in Fig.2. The input matching network is found using the input impedance of IDCLNA which is expressed in Eqn (1) [3],

$$Z_{in} = \frac{1}{j\omega_0 C_t} + j\omega_0 L_t + \left(\frac{g_m}{C_t} \right) L_s \quad (1)$$

Where g_m is the transconductance of main transistor. ω_0 is the angular frequency at resonance. The total inductance is expressed as in Eqn (2),

$$L_t = L_g + L_s \quad (2)$$

L_g and L_s are the gate and source inductances. The total capacitance is given in Eqn (3),

$$C_t = C_{gs} + C_d \quad (3)$$

C_{gs} and C_d are the gate-to-source and additional capacitances.

The gate to source capacitance C_{gs} is calculated by Eqn (4),

$$C_{gs} = \frac{2}{3} W_{opt1} L C_{ox} \quad (4)$$

The input impedance is to be matched to 50Ω and equating real and imaginary terms in Eqn (1) to find the values of source inductor L_s , gate inductor L_g and the capacitance C_d . The parameters L_s , L_g and C_d are adjusted to obtain the perfect input impedance matching.

B.Active Inductor design

The design of active inductor is studied using gyrator-C circuit given the figure 4.3. When one port of the gyrator is connected to a capacitor, the network is called the gyrator-C network. A gyrator-C network is said to be lossless when both the input and output impedances of the transconductors of the network are infinite and the transconductances of the transconductors are constant. Gyrator-C networks can therefore be used to synthesize inductors

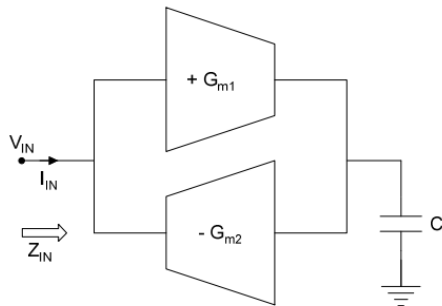


Fig. 3 Gyrator- C active inductor

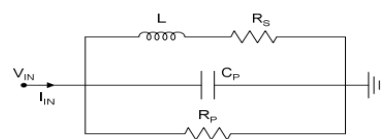


Fig. 4 Equivalent Gyrator-C circuit

The equation for inductance for gyrator-C circuit is given by:

$$L = \frac{C}{gm_1 gm_2} \quad (5)$$

The equation for quality factor is given by :

$$Q = \left(\frac{wL}{R_s} \right) \left(\frac{R_p}{R_p + R_s \left(1 + \left(\frac{wL}{R_s} \right)^2 \right)} \right) \left[1 - \frac{R_s^2 C_p}{L} - w^2 L C_p \right] \quad (6)$$

The fig5 shows the actual implementation of the active inductor. The negative transconductance is implemented by the transistor M_1 in common-source configuration. The transistors M_3 - M_4 - M_5 form a positive transconductance where the simple current mirror circuit is obtained by M_4 - M_5 is used to invert the conductance. The transistor M_6 - M_7 - M_8 are used for the biasing purpose. M_4 is the transistor is used to externally handle the block of inductor. A improved performance can be obtained by the minimum number of MOS transistors drain terminals. The cascade stage implemented by M_2 , is responsible for reducing the parasitic series resistance. Thus this improves the quality factor. The Q factor can be further increased by implementing the cascade stage.

But this can be really problematic as this may cause unnecessary poles and zeros in the signal path. The cascade gain can be further be increased by using proper feedback amplifier to regulate the gain of M_{10} . By adding additional gain stages it will result in regulated and multi regulated cascade technology(MRC).

A simple inverter stage of M_{10} can be used to obtain the regulated cascade stage. The signal path is M_1 to M_5 . Moreover the regulated stages do not degrade the high frequency response of the inductor as the signal path is still from M_1 - M_5 . The cascade gain can be still controlled in any of the ways. Hence the Q factor of the inductor can be tuned independently. C_1 and G_{o1} can be use dto independently adjust the inductance L_{eq} and its series resistance R_s .

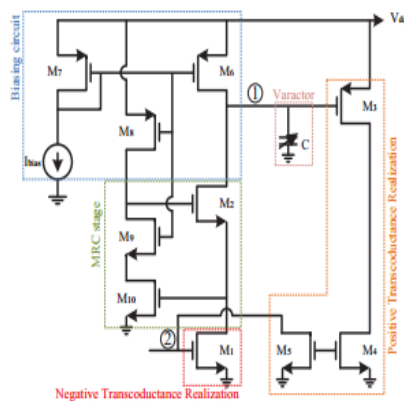


Fig. 5 Circuit implementation of active inductor (AI)

$$C_1 = C_{i1} + C \quad (7)$$

Where, C_1 – output capacitance of M_1

C_{i1} – input capacitance of M_1

C – inductance tuning capacitance

$V_{gs} + V_{dsat}$ is the actual voltage required for the proper circuit operation.

V_{dsat} is the minimum voltage required to keep the transistor in saturation.

$V_t \leq V_i \leq V_{dd} - 2V_{dsat}$ is said to be the voltage swing at the input. We can see that only two transistors contribute to the input noise, thus, the circuit would have less noise.

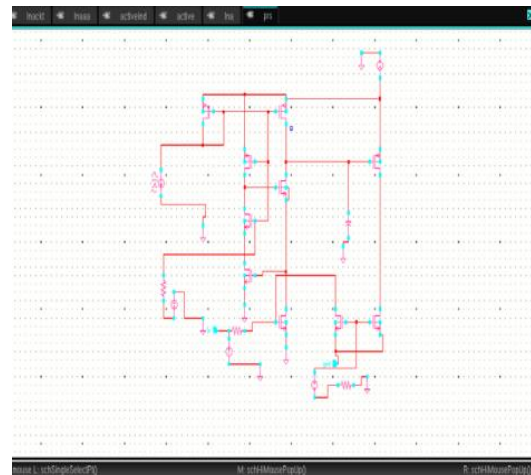


Fig 6 Active inductor

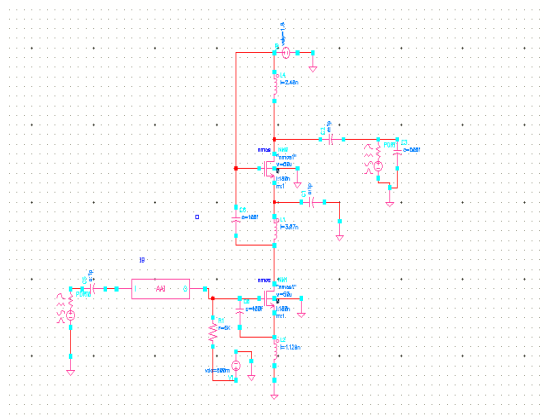


Fig 7 Proposed LNA using active inductor

IV. OUTPUTS

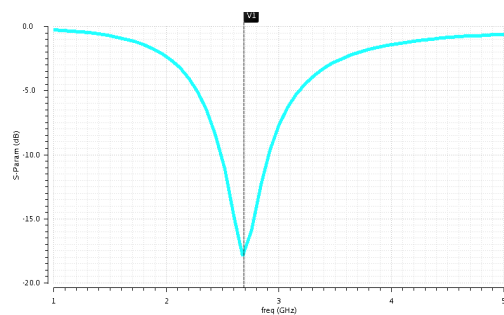


Fig 8 Input Return Loss of Current Reused LNA (S11)

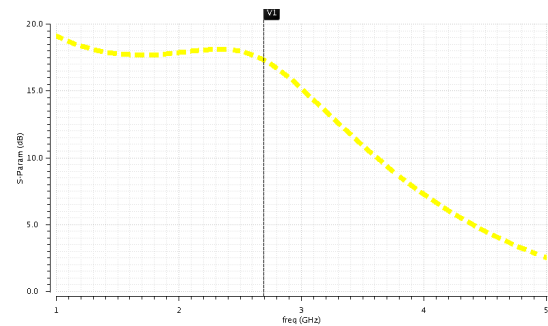


Fig 8 Gain of Current Reused LNA (S21)

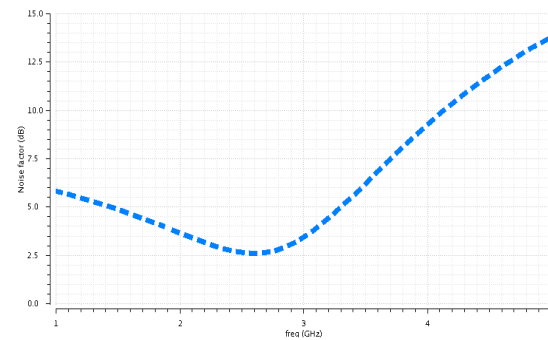
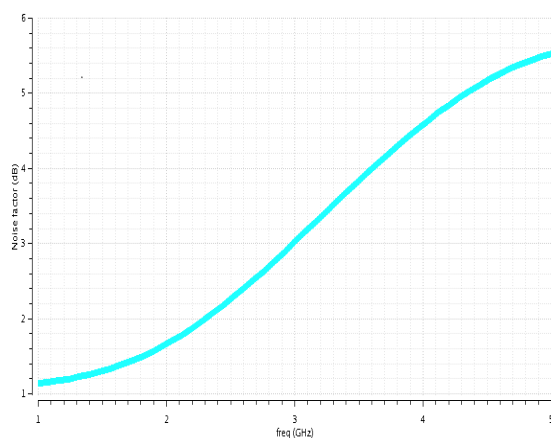


Fig 9 Noise Figure at the Output (nf2)



Minimum Noise Figure (NFmin)

V. CONCLUSIONS

The presented LNA uses the current-reuse technique in order to improve performance. The gate inductor of LNA is replaced by an active inductor in order to reduce the integrated area. This LNA shows a proper input matching at 2.6GHz. The gain of the proposed LNA is about 17.32 dB, noise figure is 2.67dB, input return loss is -17.7823 dB and power consumption is about 5.856 mW. It can be used for small satellite ground stations.

This work can be further improved in future by scaling down to less than 180nm which promises sharper gain, increase in performance and lesser integrated area. All the passive inductors in LNA can be replaced by active inductors which can further reduce the chip area and noise figure. The LNA can also be used in wide range of frequencies.

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REFERENCES

1. E. V. V. Cambero, R. R. Munoz, I. R. S. Casella, A. J. SguareziFilho, H. X. Araujo and C. E. Capovilla, 2017, 'CMOS Low Noise Amplifier Topology Using Compact Wu Folded Active Inductor', IEEE LATIN AMERICA TRANSACTIONS, vol. 15, no. 10, pp.1827-1833.
2. S.Manjula and M.Malleswari , 2017, 'Design of CMOS High Linear Low Noise Amplifier for Small Satellite Ground Station', National Conference on Small Satellite Technology and Applications.
3. Hadi Ghasemzadeh Momen, Motin Yazgiand RamazanKopru, 2016, 'A low Loss, Low Voltage, High Q Active Inductor With Multi Regulated Cascaded Stage For RF Applications', Telecommunications and Signal Processing (TSP) 2016 39th International Conference, Egypt, pp. 291-294
4. HardikSathwara and Kehul Shah, 2015, 'Design of Low Power CMOS Low Noise Amplifier Using Current Reuse Technique', 5th Nirma University International Conference on Engineering (NUICONE), India
5. SaberKaria, ShKazemia, V. Shirmohammadlia, M.C.E. Yagoubb , 2016, 'gm-Boosted Flat Gain UWB Low Noise Amplifier With ActiveInductor-Based Input Matching Network ', ELSEVIER Integration, the VLSI journal 52(2016)323-333
6. Rajan Kumar, DivyeshSachan, Sonu Singh Yadav, Ankit Kumar Sihara and Prasanna Kumar Misra, 2017, 'Design of Active Inductor at 2.4 GHz frequency using 180 nm CMOS Technology', 4th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), 978-1-5386-3004-4/17/\$31.00

7. 7. K.Saravanan, G.Vishnu Vardhan Rao, P.Bala Venkateswarlu, M.R.Bibn, "Power Efficient Clock Pulsed D Flip Flop Using Transmission Gate" Int journal of control theory and applications, PP 3607-3614, VOL 9(9), 2016.
8. V.Prabhu, Jency Rubia J, Gopal B.G (2015), "Analysis, Design and Implementation of 4-Bit Full Adder using FinFET ", Journal of Convergence Information Technology, 2015 Volume 10 Issue 2.

