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A 60GHz High Gain CG-CG Current Reuse Low Noise Amplifier for Inter Satellite Communication for Space

Rashmi S B[1], Dr. Siva S yellampalli[2]

[1]*Dept. of ECE, DBIT, Bangalore, India*
[2]*VLSI and Embedded Systems, UTL Technologies, Bangalore, India*
**Corressponding Author and Email:*
**[1]sbrashmishreedhar@gmail.com*
**[2]Siva.yellampalli@gmail.com*

Abstract

In this paper a novel design of 60GHz Low Noise Amplifier (LNA) using common gate (CG) - common gate (CG) current reuse technique is presented. The proposed technique enhances the performance of LNA using pseudo CS topology. The implementation is carried out by using 90nm CMOS processes. The proposed architecture can give a peak gain > 10dB at 60GHz. The LNA exhibits a noise figure of 1.00634dB at 60GHz and a reverse isolation of -28.48dB. The circuit ensures the power dissipation of 16.5mW with 1.8V supply. The LNA achieves the S11 of -10.19dB. In this design power dissipation and gain parameters are enhanced by using pseudo CS current reuse architecture.

Keywords—class AB, 60GHz, power amplifier, PAE, transceiver, input match

1. Introduction

In today's world, plenty of satellites are launched in the space, once the satellites complete their life cycle they are treated as garbage in space. Day by day the amount of space garbage is increasing leads to collision of junk satellite with working satellite. This can be avoided by enabling the inter satellite communication in the space. This is realized by millimeter wave CMOS transreceiver [4] which works at 60GHz [7]. The band of 57GHz to 63GHz is selected to perform inter satellite communication at the data rate more than 4-8 GB/S. At the space the distance between transmitter and receiver can be enhance due to vacuum. One more important application of this band is it is an unlicensed frequency band worldwide. In this paper an attempt is made to realize the mm-wave analog component which works at unlicensed 60GHz band. To design 60GHz band transceiver varieties of analog components need to be designed. Among them at receiver first critical active component is Low Noise Amplifier (LNA). The LNA should desire to have high gain, low power, high reverse isolation and reduced noise figure. Due to the high operating frequency of 60GHz, the millimeter-wave CMOS LNA mainly suffers from reduced gain increased power dissipation and very high noise figure. To achieve minimum noise figure common gate configuration is selected. In CG architecture noise figure is basically independent of operating frequency, on the other hand CG architecture mainly suffers from low gain and increased power dissipation. To ensure high gain with reduced power dissipation current reuse architecture [1] is preferred. This architecture is called as current reuse because the bias current of driver is reused to bias the load transistor. Since the same current is used, the power dissipation is comparatively less. This architecture has two transistors, one is driver and second one is load transistor. Depending on the configuration used in both the transistor type this architecture is broadly classified in to 4 categories.

- Common Source-Common Source (CS-CS).
- Common Source- Common Gate (CS-CG)
- Common Gate- Common Source (CG-CS)
- Common Gate- Common Gate (CG-CG).

The CS-CG is basically a normal cascade it has the advantage of increased gain but it mainly suffers from linearity issues at millimeter wave frequency. To get higher gain and low power dissipation CS-CS architecture [10] is used. Here both the transistors are biased in common source configuration. This architecture has following drawbacks. I. difficult to balance tank circuits. II. Reverse isolation of CS stage is considerably low. III. Increases the stability issues. IV noise figure of CS LNA at millimeter frequency is considerably high. In CG-CS topology [11], driver is biased in common gate configuration as driver is mainly contributed for gain this is suffering from low gain. To get the desired gain number of amplification stages need to be increased. This in turn increases the area requirement. In this paper an attempt is made to design and implement the CG-CG architecture for higher gain, by using the concept of proposed pseudo CS circuit. Low power is ensured by current reuse architecture and the desired reverse isolation is achieved by CG configuration. The main advantage of CG topology is noise figure is independent of operating frequency. Thereby even at millimeter wave frequency the noise figure is preserved. The proposed circuit is implemented by using cadence virtuoso 90nm CMOS. The proposed single stage amplifier is enough to get the desired gain. To achieve higher gain number of stages can be cascaded.

2. Design Parameters Of Low Noise Amplifier

2.1 Power Gain:

Power Gain is defined as

$$G = \frac{P_L}{P_{in}} = \frac{power\ dissipated\ at\ load}{power\ delivered\ to\ input} \quad 1$$

Transducer gain G_T is defined as

$$G_T = \frac{P_L}{P_a} = \frac{power\ dissipated\ in\ load}{power\ available\ from\ source} \quad 2$$

Available gain G_A is defined as

$$G_A = \frac{P_{AT}}{P_a} = \frac{power\ available\ from\ two\ port\ network}{power\ available\ from\ source} \quad 3$$

Linearity: The linearity issue existed depending the type of modulation scheme incorporated in modulation. In transmitter section if the amplitude modulation is incorporated then the power amplifier need to be linear region. In power amplifier the trade-off exist between efficiency and linearity. Assume that the input given to designed power amplifier is amplitude modulated wave($V_{in}(t)$), if the power amplifier is highly non linear in nature. Then output of the amplifier V_d is given by

$$V_d = AV_{in}(t) = a_1 V_{in}(t) + a_2 V^2_{in}(t) + a_3 V^3_{in}(t) \quad 4$$

This non linearity need to be minimized in amplitude modulated output for recovering the information present in the envelop of the output.

To get minimum noise figure using transistor the power reflection coefficient should match with

Γ_{out}^* and load reflection coefficient should match with Γ_{out}

$$\Gamma_s = \Gamma_{opt}$$

$$\Gamma_L = \Gamma_{out}^* = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right) \quad 5$$

The overall performance of power amplifier is determined by calculating GT. The proposed power amplifier MOSFET works at a power supply voltage of 1.8V. It is designed to deliver a output power of 10mW. It ensures the P1dB of 11.7dB and Γ_{opt} of 0.815+j0.2209. The stability of the design is ensured with the equation given 6 and 7.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} = 1.57 > 1 \quad 6$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} = 0.19 < 1 \quad 7$$

2.2 Noise Figure

The one more component which need to be considered in designing low noise amplifier is its noise figure. Generally it is difficult to design an amplifier which gives low noise figure and high gain. Considering this issue tradeoff is done between gain and noise figure to design consider constant gain circle and circle of constant noise figure. The noise figure is defined as

$$F = F_{\min} + \frac{R_N}{G_S}|Y_S - Y_{opt}|^2 \quad 8$$

Where

Ys= source admittance
Yopt=source admittance results in minimum noise figure
Fmin=minimum noise figure when Ys=Yopt
R_N= Equivalent noise resistance
Gs= real part of source admittance

The desired noise figure N is defined as the

$$N = \frac{F - F_{\min}}{\frac{4R_N}{Z_0}}|1 + \Gamma_{opt}|^2 \quad 9$$

Fmin, Γopt, RN are provided low noise transistor manufacturers for desired frequency.

3. Transistor Model

In RFIC's design transistors are normally biased at a constant drain current density. The transistor's power consumption normally a resultant of current and drain-source voltage V_{DS}. Further VGS is applied to achieve desired current density and it has no effect on dissipated dc power.

3.1 MOSFET high frequency performance

To characterize transistors RF performance at a chosen bias point following figure of merit are employed.

- Cut-off frequency f_T
- Maximum oscillation frequency f_{max}

An evaluation of f_T and f_{max} performance for selected MOSFET from gpdk45 library. Figure 1 depicts the f_T is plotted against different gate-source voltage Vgs. Figure 2 shows the current density is plotted against cutoff frequency f_T. This plot ensures the maxima of fT is achieved for a current density of mA/um. This proves the selected MOS can yield a low power consumption and high frequency gain.

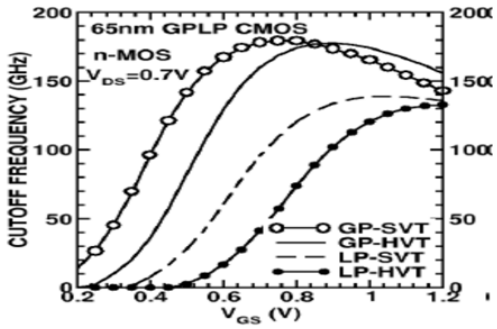

Fig. 1 f_T versus gate source voltage

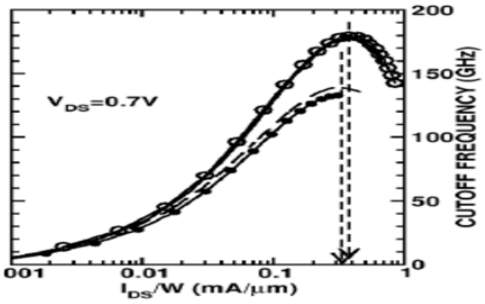

Fig. 2 current density versus cut-off frequency

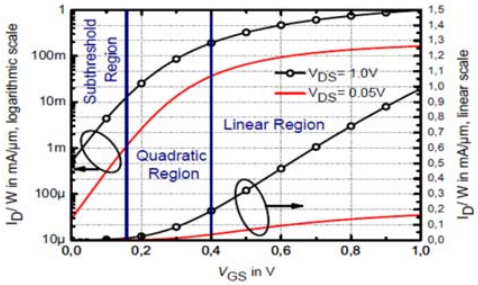

Fig. 3 Normalized DC transfer characteristic of 45nm nmos1v n-channel MOSFET based on simulation using gpdk models

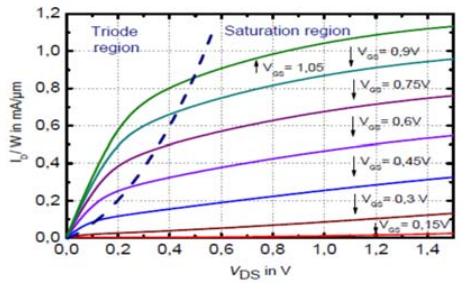

Fig. 4 output characteristics of 45nm nmos1v n-channel MOSFET based on the simulation using gpdk models.

Figure 3 shows the simulated DC transfer characteristics of a nmos1v n-channel MOSFET with L=45nm gate length. The graph depicts the pinch-off voltage of MOSFET is around 250-280mV.

Figure 4. output characteristics of 45nm nmos1v n-channel MOSFET based on the simulation using gpdk models. Here to bias the power amplifier in class AB configuration it need to be biased at Vgs=0.4V and Vds=1V which yields a current density of 500uA/um.

4. Cg-Cg Current Reuse Lna Topology

The circuit diagram of CG-CG current reuse architecture is as depicted in figure 5. In this architecture both the driver and load are designed using common gate configuration. In this design input is applied at the source of the driver transistor. Output of the driver is coupled to the source of load transistor via inductor Lc. The main purpose of this coupling inductor is to nullify the effect of miller capacitance C_{gd} of M1.This Cgd is divided between gate and drain side. The capacitance at the gate is compensated by gate inductor and capacitance at drain is nullified by Lc. For designing the 60GHz LNA a supply voltage of 1.8V is selected.

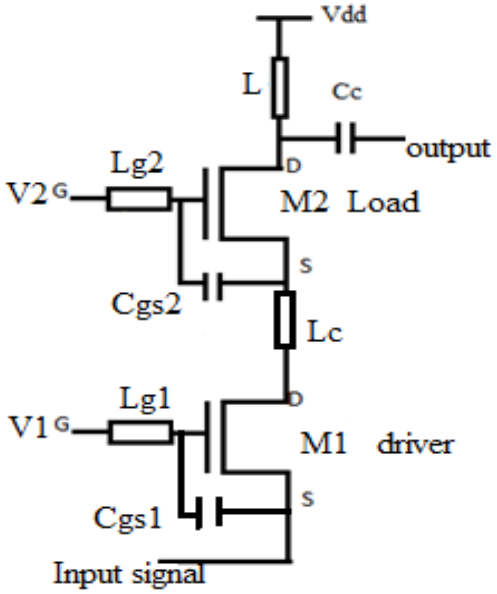

Fig. 5 CG-CG current reuse topology

The important advantage of CG [3] is its reduced noise figure and improved reverse isolation. In this design gain can be enhanced by using pseudo CS topology. The meaning of pseudo CS is, the driver stage is connected as common gate configuration but internally working as common source which in turn enhances the gain of the single stage LNA. To design this low noise amplifier nmos1v MOSFET is considered in gpdk90 technical library. The single stage amplifier can yield a maximum gan of 10dB and noise figure of 1dB. An RF input is applied to source of driver transistor, and an inductor is connected at the gate of the MOS. At the desired frequency this inductor needs to be resonated with gate to source parasitic capacitance C_{gs} of driver transistor. C_{gs} and gate inductor L_g forms a series resonance. At the series resonating frequency, the impedance offered by the network is very minimum. Thereby the input applied at the source is coupled to the gate via series resonating network. Thus even with common gate topology this circuit is inherently behaves as common source

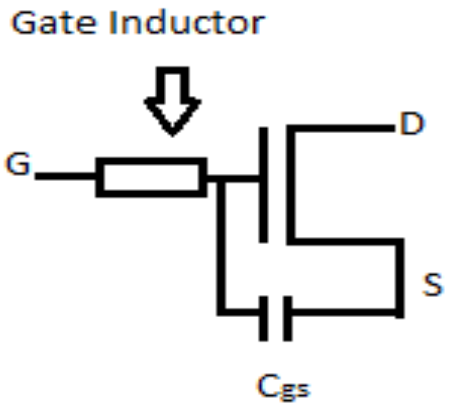

Fig. 6 Pseudo CS topology

The circuit diagram of pseudo CS circuit is depicted in figure 6. At resonating frequency

$$\frac{i_2}{i_1} = \frac{f_T}{f_0} \quad 10$$

Where i_2= output current of MOS

i_1= input current of MOS
f_T= unity gain frequency of MOS at 90nm
f0= operating frequency

For 90nm MOS minimum gate length at unity gain frequency is 120GHz[1] and design frequency selected is 60GHz. Thereby output current is minimum twice the input current.

4.1 Small Signal Model of the proposed circuit

Small signal model of the figure 1 is shown in two sections the small signal model of the first section or driver section is as depicted in figure 7. The input impedance [5], [8] of the circuit is given by.

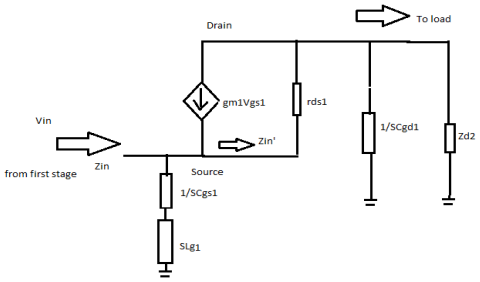

Fig. 7 Small signal model part I

$$Z_{in} = Z_{in}^{'} \parallel [1/SC_{gs1} \parallel SL_g] \quad 11$$

$$Z_{in} = \frac{Z}{1 + g_{m1} r_{ds1}} \parallel [1/SC_{gs1} \parallel SL_g \quad 12$$

The small signal model of the second part or driver section is shown in figure 8.

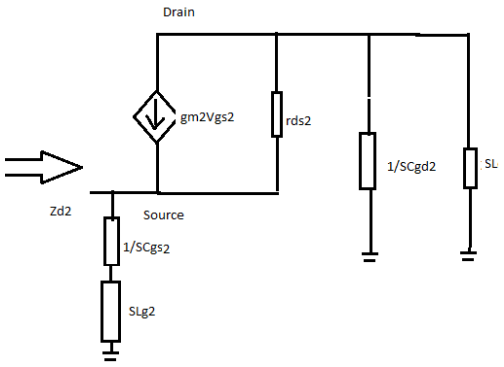

Fig. 8 Small signal model part II

From figure 4 impedance Zd2 is given by equation 13.

$$Z_{d2} = [SL_{g2} + \frac{1}{SC_{gs2}}] \parallel \frac{\frac{1}{SC_{gd2}} \parallel SL_d \parallel r_{ds2}}{1 + g_{m2} r_{ds2}}. \quad 13$$

The output impedance is given by equation 14

$$Z_{out} = Z^{'} \parallel SL_d \parallel \frac{1}{SC_{gd2}} \quad 14$$

Where

$$Z^{'} = Z + g_m r_{ds2} Z + r_{ds2} \quad 15$$

5. Measurement Results

The designed CMOS CG-CG LNA was tested and results are measured with virtuoso analog and digital environment 90nm technology. The measured S-parameters are shown in Figure. 9. The maximal power gain is 10 dB at 60 GHz with a 3-dB bandwidth span from 57 to 64 GHz. The reverse isolation is better than -28.48dB. The input return loss is -10.19 dB and output return loss is - 5 dB at 60 GHz. The measured noise figure reaches a minimum of 1.00634 dB at 63 GHz, as depicted in Figure 10.

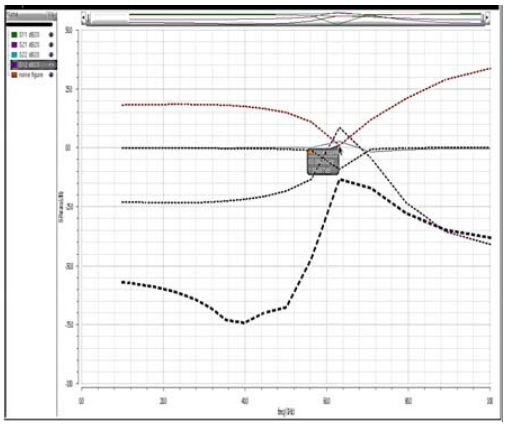

Fig. 9 S-parameter analysis

The gain of the circuit is given by equation 16

$$A_V = \frac{V_{out}}{V_{in}} = \frac{1 + g_m r_{ds}}{r_{ds} + g_m r_{ds} SL_s + SL_s + Z} Z \quad 16$$

Where

$$Z = [SL_{g1} + \frac{1}{SC_{gs2}}] \| \frac{(\frac{1}{SC_{gd2}} \| SL_d) + r_{ds2}}{1 + g_m r_{ds2}} \quad 17$$

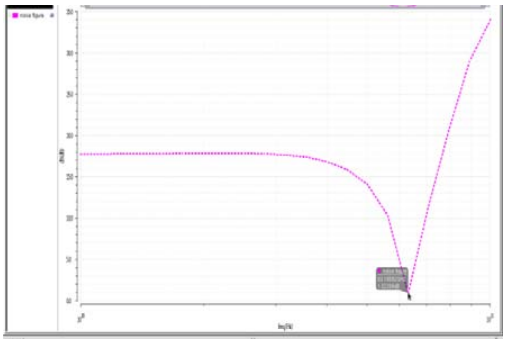

Fig. 10 Noise figure of the proposed circuit

The important advantage of the proposed architecture is its reduced noise figure. The reduced noise figure of 1.007dB results in improved performance. In the proposed design there are 4 inductors used in the design, the effect of inductance on noise figure are discussed. The effect of gate inductance on noise figure is shown in figure 11. Figure shows that noise figure is optimum at gate inductance of driver transistor is 3.72nF.

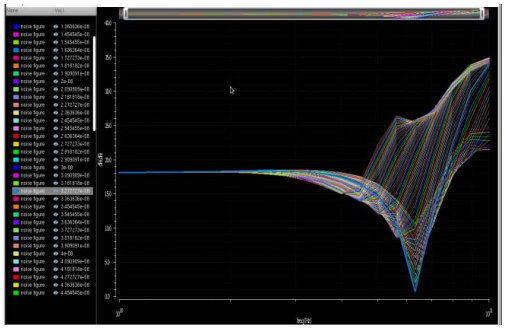

Fig. 11 Effect of gate inductor of driver MOS on noise figure

The effect of noise figure on gate inductance on load MOS is as depicted in figure12. The noise figure is minimum at gate inductance of load transistor of 6.13nF

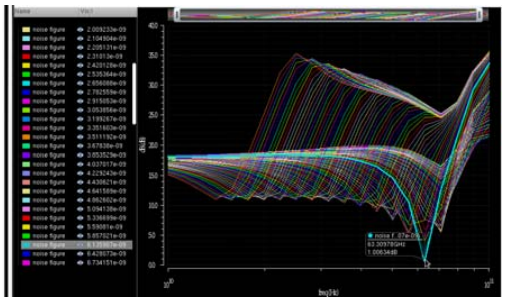

Fig. 12 Effect of gate inductor of load MOS on noise figure

The effect of noise figure on load inductance is as depicted in figure 13. The figure 13 clearly demonstrates that noise figure is independent of load inductance.

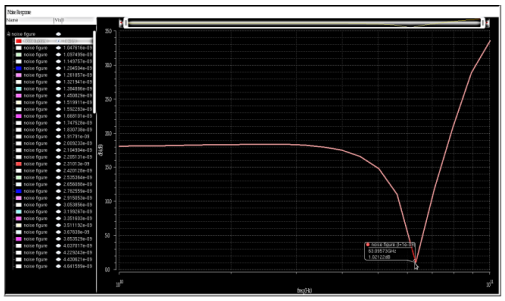

Fig. 13 Effect of load inductor on noise figure

The effect of different inductors on noise figure depicts that there is no effect of load inductance on noise figure. Noise figure is entirely depending on gate inductance of driver and load MOSFETs. The gate inductors are designed to have optimized noise figure.

The transient and ac analysis of the proposed circuit is depicted in figure 14. Circuit gives the maximum voltage gain of 27dB at 60GHz. The input and output of the proposed LNA is 1mV and 25mV measured from spectre virtuoso analog and digital environment.

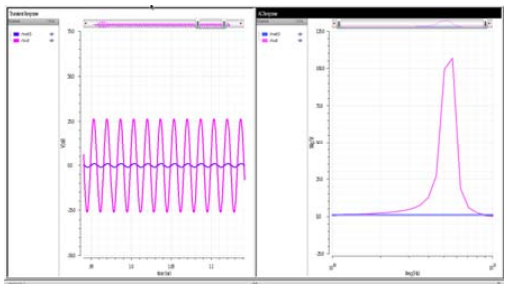

Fig. 14 Effect of gate inductor of driver MOS on noise figure

6. State Of Art Comparision

Table 1 comparative study of different LNA at 60GHz

Vdd	Ref	Frequency of Operation	Gain In dB	NF	Reverse isolation	Number of stages	Power In W	Technology
2	[9]	60GHz	28	4.1dB	-	differential	-	130nm
-	[8]		20	3.5dB	-12dB	four	-	150nm
-	[7]		12	-	-	-	-	350nm
	[6]		10.5	4.73~0.83dB	-42.6	three	14.1m	90nm
1.2	[5]		18	4.7dB	-19dB	three	28.32m	90nm
1.2	[3]		20.6	4.9dB	-	three	33.3m	65nm
1.5	[2]		22	5.2dB	-22.4dB	two	16.8m	65nm
1.7	[1]		5.1	7dB	-25dB	Single	18.5m	90nm
1.5	This work	60GHz	10	1.002 dB	-28.48dB	single	16.5m	90nm

The advantage of the proposed architecture is reduced noise figure of 1.00634dB at the operating frequency of 60GHz. Even at microwave frequency of 60GHz and 6GHz bandwidth is exhibiting a least noise figure since the architecture of common gate topology is independent of operating frequency. The common gate topology also offers one more advantage of improved reverse isolation the reverse isolation of LNA is at least < -15dB. The designed LNA will provide a peak reverse isolation of -28.48dB at 60GHz. Here both the driver and load transistors are biased in CG topology mainly suffers from gain. In this design gain is maintained to a maximum of 10dB. Further it can be enhanced by increasing number of stages

7. Conclusion

In this paper a detailed implementation of 60GHz CG-CG current reuse topology is done. The proposed circuit is reports a peak gain of 10dB. The noise figure of the proposed system is 1.00634dB. The reverse isolation of this system is -28.48dB it is expected to be less than -15dB. Finally comparison is done with different 60GHz LNA for various design parameters such as noise figure, reverse isolation, gain as shown in table 1.

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