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Design and Analysis of Adiabatic Vedic Multipliers

Premananda B.S[1], Nagesh N. Nazare[2], Pradeep S. Bhat[3], Nayana R. J[4].

[1,2,3,4]*Dept. of TCE, R. V. C. E., Bengaluru*
Corresponding author and e-mail:
[*1]*premanandabs@gmail.com*
[*2]*nagesh.nazare0831@gmail.com*
[*3]*psbhat1996@gmail.com*
[*4]*nayanarjambhe@gmail.com*

Abstract

Power utilization is one of the most important criteria in present day DSP systems. This problem can be efficiently resolved by using Adiabatic logic circuits, where the power is recycled back to the source instead of dissipating it as heat. Adders and Multipliers are basic building blocks of various systems ranging from signal processing to cryptography, and hence their efficient low power design is very essential. In this paper, Urdhva-Tiryakbhyam Sutra, a Vedic algorithm is used to realize the multipliers. Further, a modification to the existing Vedic multiplier is provided. An N*N traditional Vedic multiplier uses four N/2 -bit multipliers and three N-bit adders, whereas a N*N proposed Vedic multiplier requires four N/2 -bit multipliers, one N-bit adder and two 2N-bit adders. Static CMOS and Adiabatic designs are implemented in Cadence Virtuoso with 180 nm technology node and functionally verified in Spectre-simulator. As the number of transitions are reduced in modified architecture, the power consumption is less. It is observed that in modified Vedic architectures, a Power saving factor of 9.75 and 9.83 is obtained for 4x4 and 8x8 multipliers, respectively.

Keywords—*Adiabatic Logic (AL), Kogge-Stone Adder (KSA), Urdhva-Tiryakbhyam (UT), Power Saving Factor (PSF)*

1. Introduction

The demand for portable and small sized devices has been growing exponentially in the last few decades. Low power IC design techniques need to be used to solve the problem of minimum battery capacity of these devices, specifically in portable devices. Many low power design techniques have been proposed at different hierarchical levels. Some of the new recent research trends are Adiabatic logic circuits, Reversible logic circuits, Quantum cell-dot Automata, and others. In Reversible logic technique, logic gates have one to one mapping between input and output, and logic operation can be derived reversibly [1]. Quantum cell-dot Automata technique uses polarized charge propagation to transfer the information from one cell to another [2].

Adiabatic Logic (AL) is the one of the promising technique to conserve the energy in digital and analog ICs [3]. The term "Adiabatic Logic" comes from Thermodynamics, which refers to a process that occurs without any energy transfer. These circuits recycle or restore the energy back to the source [9]. In these circuits, the MOSFETs are turned ON only when there is no potential difference across them, and turned OFF only when there is no current flowing through them. To attain this condition, AL Circuits use constant current charging from the power supply, in contrast to the static CMOS circuits which use constant voltage charging from a fixed DC power supply. AL Circuits are operated with an oscillating power-supply which is combination of power and clock, called as a Power-clock. They are operated with one or more than one power clock depending on the type of Adiabatic family [4]. Positive Feedback Adiabatic Logic (PFAL) uses four-phase power-clock ω_0, ω_1, ω_2, ω_3, each with 90^0 phase-shift. Each phase of the power clocks gives outputs at that interval of time. The output is valid only in a particular interval. Hence, to drive a chain of cascaded Adiabatic circuits the circuit needs multiple-phase clocking. Multiple-phase power clock also increase complexity of the clocking network [5].

For an Adiabatic system energy dissipation can be characterized using Equation (1), where R is the resistance of the circuit consisting of the on resistance of transistors in the charging path, CL represents the load capacitance and V represents the supply voltage. By increasing the rise and fall time T, large amount of energy can be saved [5].

$$E_{diss} = \left(\frac{RC_L}{T}\right) C_L V^2 \quad (1)$$

Adiabatic Circuits have two types of losses, viz., frequency dependent and frequency-independent. Losses which are dependent on the operating frequency are called Adiabatic Losses, and can be minimized by using an efficient design technique. Losses which are independent of operating frequency are called as Non-Adiabatic Losses, which cannot be avoided. Two approaches in Adiabatic Logic are Partial/Quasi Adiabatic Circuits (QAC) and Fully Adiabatic Circuits (FAC). QAC has non-adiabatic losses, whereas non-adiabatic losses are constrained in FAC. 2N-2P [10], PFAL and Efficient Charge Recovery Logic (ECRL) are the prominent techniques present in QAC. PFAL shows the lowest energy consumption compared to other techniques [3]. PFAL is a Dual-rail circuit, consisting of a latch constructed using nMOS and pMOS transistors, as shown in Fig. 1. PFAL is recognized for efficiently avoiding logic level degradation on the output nodes.

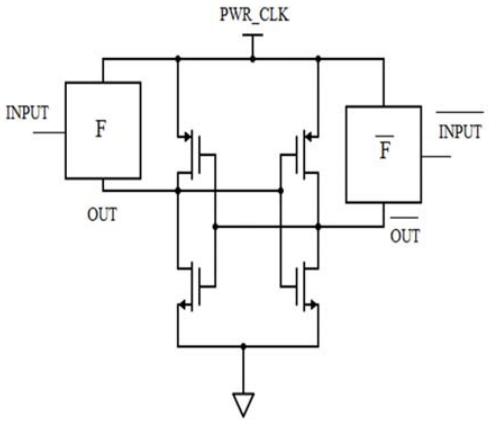

Fig. 1 Schematic of PFAL Circuit

PFAL also follows the static CMOS design flow, hence, ease the design process. PFAL has inherent Micro-pipelining scheme. The data in Adiabatic circuits is processed and handed over in a pipelined manner. The four intervals in each Power-clock cycle of PFAL circuits, illustrated in Fig. 2 are explained:

- Evaluate (E): Outputs are calculated from the steady input signals.
- Hold (H): Outputs are retained stable to provide the next gate with a stable input.
- Recover (R): Energy is recovered in this interval.
- Wait (W): Symmetric signals are easier to generate; thus, this interval is inserted.

Adders and multipliers are the fundamental arithmetic blocks in Multiply and Accumulate (MAC), Computation-Intensive Arithmetic functions (CIAF), Arithmetic and Logic Unit (ALU) and in many Digital Signal Processing (DSP) applications such as convolution, Fast-Fourier Transforms (FFT) and filtering. Multiplication operation requires relatively larger processing time and resources than addition. The speed, power utilization and desired performance of a multiplier is very critical in signal processing and image processing systems of portable devices. A plethora of high-speed algorithms and their implementations are proposed in [4].

Vedic algorithms are one of the fastest ways of performing an arithmetic calculation, with simple principles and rules. Multiplication can be performed using Urdhva-Tiryakbhyam sutra (vertically and crosswise), which is one among the 16 sutras proposed in Vedic literature [4]. Multipliers contain adders as one of the basic component. Hence, an efficient multiplier requires an efficient adder.

Parallel Prefix Algorithm (PPA) is one of the proficient way of implementing an adder with better trade-off in speed, area and power. There are several PPA adders such as, Kogge-Stone Adder (KSA), Han-Carlson Adder, Brent-Kung Adder, Sklansky Adder, Knowles Adder, and Ladner-Fisher Adder, which can be used for the implementation of the multiplier. KSA prefix tree is considered as the fastest algorithm, as it takes only $\log_2 N$ logic levels. Carry select adders are fastest adders [11] but has more delay compared to PPA. High-performance applications use KSA for calculation of higher bit-widths [6]. Hence, in this work, KSA is used for the designing the multiplier.

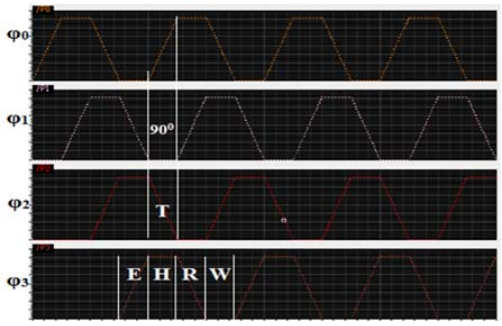

Fig. 2 Power-clock scheme in Adiabatic Logic [4]

The paper is organized as follows: Section II explains the design and implementation of Adiabatic logic gates, Parallel-Prefix adders and Vedic multipliers. In section III, results have been discussed along with the power consumption. Section IV provides conclusion and future scope of the work.

2. Design and implementation

In this section, initially, the design of Adiabatic gates (in PFAL logic) are discussed. Design concepts of Parallel Prefix Adders and their implementation are discussed in the next sub-section. In the further sub-sections, architecture of Vedic Multipliers is provided and discussed briefly. Schematic entry of the design is carried out in Cadence Virtuoso with 180 nm technology node and Spectre – simulator is used for functional verification.

A. PFAL Logic gates

PFAL is a Dual-rail circuit. It has complementary inputs and complementary outputs. The structure of PFAL contains a latch constructed using two PMOS and two NMOS transistors. The schematic of PFAL NOT gate realized in Cadence Virtuoso is shown in Fig. 3.

B. Parallel Prefix Addition

Adders should be efficient in terms of speed, power and area. Often, the maximum operating speed of a digital system depends on how fast the adders can process the data. A Parallel-Prefix Adder (PPA) can be used to overcome the carry chain problem in the serial adders. A PPA structure consists of a Pre-Processing stage, a Parallel-Prefix Algorithm tree and a Post-processing stage, as illustrated in Fig. 4. A detailed analysis of Adiabatic Parallel Prefix Adders is provided in [8].

KSA is one of the fastest algorithms to implement an adder. It solves the huge recurrence problem in digital computers using a technique termed Recursive-Doubling algorithm. Recursive-Doubling uses Divide and Conquer principle, wherein the calculation of a function is divided into two composite sub-functions whose estimation can be performed concurrently [7].

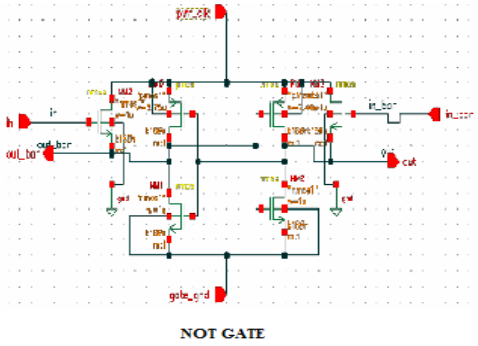

Fig. 3 PFAL NOT gate

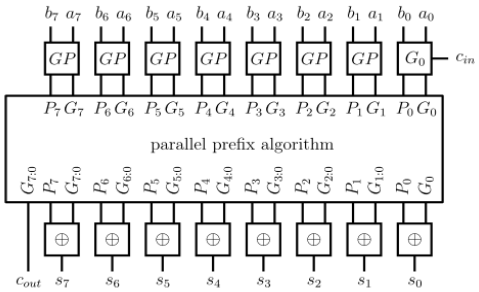

Fig. 4 Parallel Prefix Adder Structure for 8-bit Addition [4]

KSA has $\log_2 N$ stages, with a fixed fan-out of 2 at each stage, as shown in Fig. 5. This leads to several long wires that needs to be routed between the stages.

C. Vedic Multipliers

Multiplication is the process of multiplying two numbers A and B by adding A with itself B times. Time taken by the process is longer; hence many algorithms are developed to improve the speed and to minimize the area of the multipliers. The UT Algorithm, one among the sixteen sutras proposed in the literatures, is one of the proficient algorithms. It is efficient in terms of power consumption, delay, and resources. Subsequently, the partial products are simultaneously calculated. In this algorithm, partial products are obtained by ANDing each bit of multiplier and multiplicand. To obtain final product these partial products are added.

2x2 multiplier with AL is implemented by using basic gates as shown in Fig.6. ϕ_0, ϕ_1, ϕ_2 are the power-clocks driving the cascaded system. Q_0-Q_3 is the output of the multiplier. Vedic multiplier with AL is implemented by using four 2x2 multipliers and three 4-bit adders. The schematic of 4x4 multiplication is illustrated in Fig. 7. Result of multiplication is obtained as S_7-S_0, by combining the output of all adders and 2x2 multipliers.

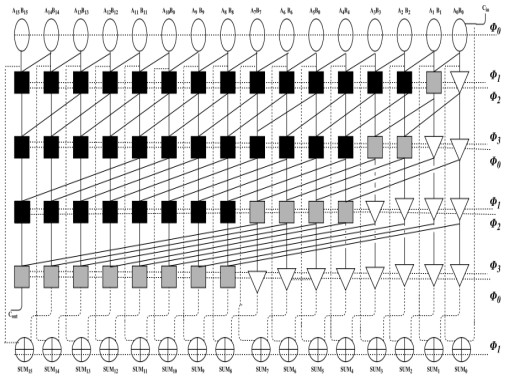

Fig. 5 16-bit PFAL Kogge-Stone Adder

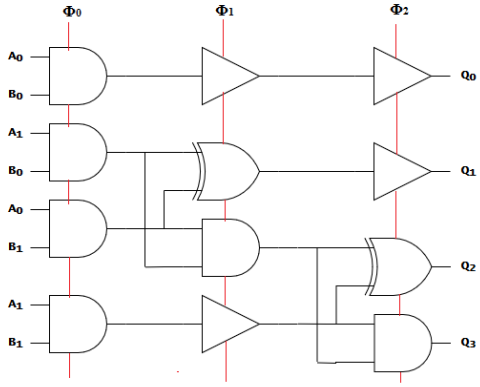

Fig. 6 2x2 Multiplier

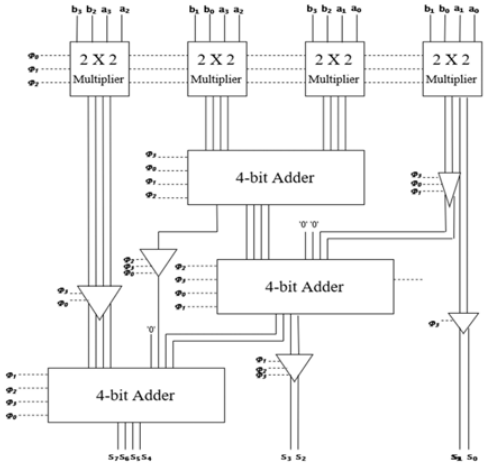

Fig. 7 4x4 AL Vedic Multiplier

The 8x8 Vedic multiplier is implemented by using four 4x4 Vedic multiplier blocks. Assume two numbers A= A_7-A_0 and B = B_7-B_0. The 16-bit obtained output S_{15}-S_0. A and B are split into two parts.

8-bit multiplicand A is made of two parts of 4 bits A_{Higher}-A_{Lower} each. Similarly, multiplicand B is made of two parts of 4-bits B_{Higher}-B_{Lower} respectively. The 16-bit result can be given as: P = A x B = (A_{Higher} to A_{Lower}) x (B_{Higher} to B_{Lower}) = A_{Higher} x B_{Higher} + (A_{Higher} x B_{Lower} + A_{Lower} x B_{Higher}) + A_{Lower} x B_{Lower}.

The final product is obtained by adding outputs of 4x4 bit multipliers. 8x8 Vedic multiplier uses four 4x4 Vedic multiplier to compute the partial products. This will divide the task by calculating partial product concurrently. Fig. 8 illustrates the schematic of 8x8 Vedic multiplier. Functionality of the multiplier is verified in Cadence Virtuoso with 180 nm technology. Fig. 9 shows the schematic entry of 8x8 Vedic multiplier in Cadence Virtuoso.

D. Modified Architectures

Architecture of conventional 4x4 Vedic Multiplier takes more execution time and also speed is less. Hence modification has been done which is illustrated in Fig. 10. In this architecture four 2x2 VM, one 4-bit KSA and two 8-bit KSA is used. Similarly, modified 8x8 multiplier can be designed, a shown in Fig. 11.

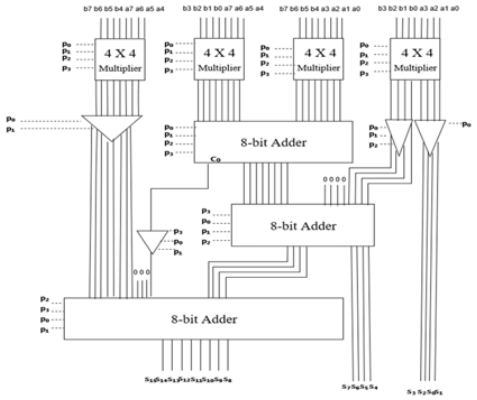

Fig. 8 8x8 Vedic Multiplier

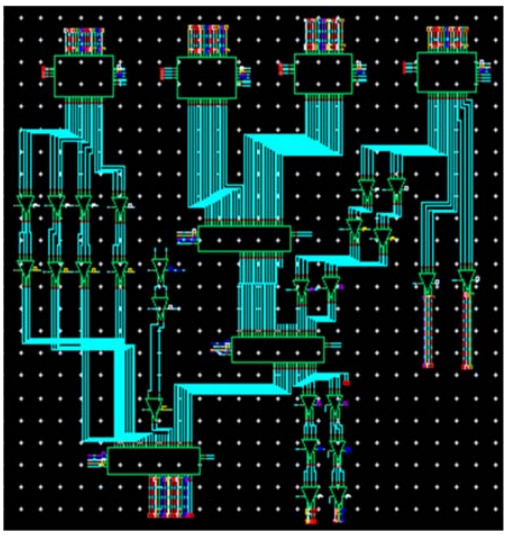

Fig. 9 Cadence Virtuoso implementation 8x8 PFAL Vedic Multiplier

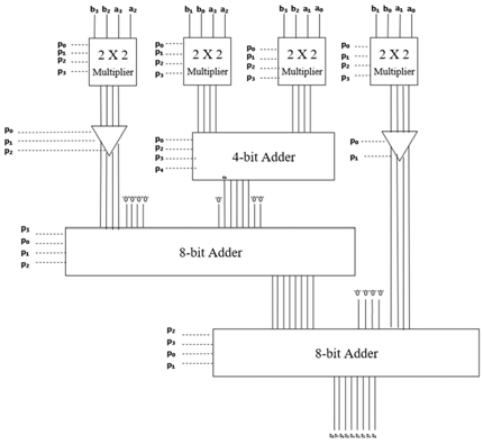

Fig. 10 4x4 Modified Vedic Multiplier

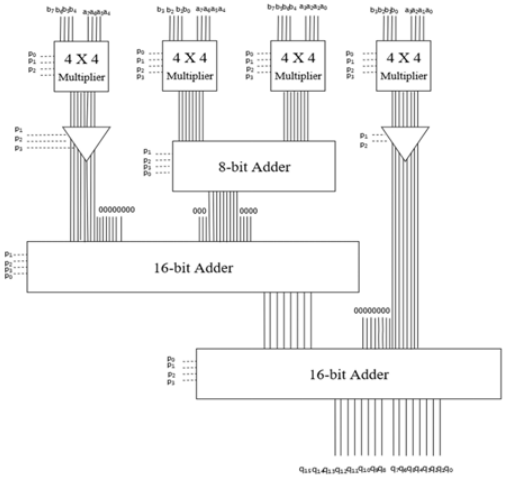

Fig. 11 8x8 Modified Vedic Multiplier

3. Results & Discussions

The schematic representation of all the multipliers is implemented in Cadence Virtuoso®, version IC6.1.4.485 with CMOS 180 nm technology. Logic level '1' as 1.8 V and Logic level '0' as 0 V represented in the tool. The design analysis and verification of circuit functionality is performed in Spectre- simulator. The input to the 8x8 Vedic multiplier is given as A = "11111111" and B = "11111111", and multiplier output obtained is "1111111000000001" as illustrated in Fig. 12. The power comparison is performed between Traditional Vedic Multiplier and Modified Vedic Multiplier. Table I and II list the power analysis of Multipliers for Adiabatic and conventional logic technique at 1 MHz frequency.

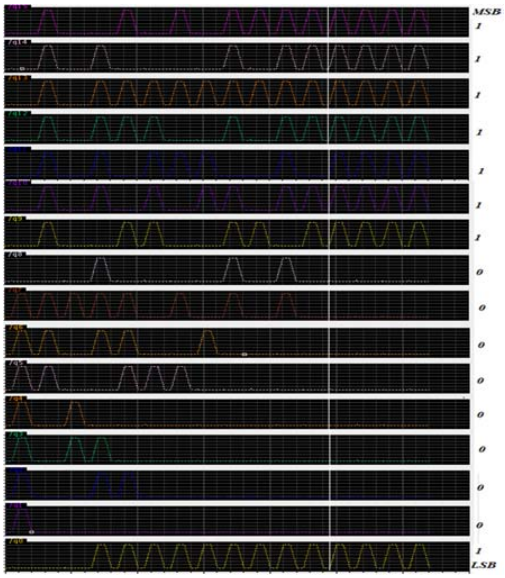

Fig. 12 Output of 8x8 Vedic multiplier

Table II explains the Power consumption of multipliers using Adiabatic and Static CMOS logic. At 1 MHz, PFAL multiplier consumes very less power compared to static CMOS multipliers. Power Saving Factor (PSF) gives the reasonable comparison of Adiabatic Circuits and static CMOS circuits, with respect to power. Equation (2) represents the formula to calculate the PSF.

$$PSF = \left|\frac{power\ dissipated\ in\ CMOS\ multiplier}{power\ dissipated\ in\ \ Adiabatic\ multiplier}\right|_{f_0} \qquad (2)$$

Power is characterized by transition of values, from 0 to 1 or 1 to 0, at each sub-block of the multiplier. As the number of transitions are reduced in Modified Adiabatic architectures, the power is reduced. It can be noted that in case of Modified Vedic Multipliers, 4x4 architecture has a PSF of 9.75 and 8x8 architecture has a PSF of 9.83 whereas in case of traditional Vedic Multipliers, it is 12.12 and 9.6. As the frequency increases, the power dissipation also increases.

Table I: Power analysis of Traditional Vedic Multipliers at 1 MHz

	Static CMOS	**PFAL**
2x2 Multiplier	510.5 nW	58.0 nW
4x4 Multiplier	26.3 µW	2.17 µW
8x8 Multiplier	62.6 mW	6.52 mW

Table II: Power analysis of Modified Vedic Multipliers at 1 MHz

	Static CMOS	**PFAL**
4x4 Multiplier	20.47 µW	2.1 µW
8x8 Multiplier	58.24 mW	5.92 mW

4. Conclusions

The essential factor in the current circuit configuration is to minimize the power dissipation of the versatile gadget and upgrade the execution of the circuit. Adiabatic Logic is one of the low-power techniques which can be used for this purpose. In this work, 4x4 and 8x8 Vedic multiplier is designed in Adiabatic and static CMOS technique. Results obtained show that the Adiabatic multipliers consume low power compared to static CMOS technique. At 1 MHz, 4x4 Modified Vedic Multiplier has a PSF of 9.75 whereas 8x8 Modified Vedic multiplier has a PSF of only 9.83. Vedic multiplier uses the efficient algorithm technique. The adiabatic implementation of these multipliers shows that there is a huge decline in power dissipation in contrast to static CMOS technique.

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