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FPGA IMPLEMENTATION OF HIGH PERFORMANCE AND LOW POWER FIR FILTER DESIGN USING ROUNDING BASED APPROXIMATE MULTIPLIER (ROBA MULTIPLIER)

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ABSTRACT— In a recent technology a multiplier is more important in all applications such as digital signal processing, image processing, cryptography application and so on. Since this all application is a most high priority in today digital world such as 3G, LTE, Tele-communication, audio and video processing. In this DSP application, the multiplier is more priority to reduce signal noise, fluctuation in all type of gadgets. In this method of ROBA Multiplier will design based on approximate multiplier with high speed yet energy efficient, and it will work both signed and un-signed multiplier without changing any parameters design. Here, we present a digit-reconfiguration finite impulse response (FIR) filter architecture are inherently pipelined and support multiplier constant multiplication (MCM) technique, it provide the results in significant manner with computation in multiplier technique. In multiplier constant multiplication (MCM) design, will not work for two way of approach, we need to designed separate signed and unsigned operation based upon the requirement, so it required more logic size, and more power consumption. In this paper, we propose an low power and low pass FIR filter design using rounded based approximate multiplier with brent kung adder to establish a high speed yet energy efficient design of DSP Signal processing application. The proposed approach is applicable to both signed and unsigned multiplications in rounded based approximate multiplier. We propose hardware implementations of the MCM to replace a rounded based approximate multiplier that based on signed operation for coefficient multiplication in FIR filter design. Finally the proposed architecture will designed in VHDL and synthesized in Xilinx FPGA S6LX9, and shown the comparison of Area, Power and Delay.

Index Terms—FIR (Finite Impulse Response), MCM (Multiple constant Multiplication).

INTRODUCTION

In recent research of digital signal processing applications to minimizing the size of hardware in all gadgets such as smart phone, tablets, wearable device, automation products and so on. In this application, to highly desired to achieve the products in minimal performance and minimization of area, and power. In this DSP application, the multiplier is the main priority to reduce signal noise, fluctuation in all type of applications. In this method a computational core of all arithmetic operation in FPGA based design, a Multiplication have more priority to sharing the arithmetic operations in DSP system. Therefore, the performance of gadgets will improving the speed and energy and also to meet a efficiency in less area and less power consumption. In this FIR Filter is very often and need to support in digital signal processing to high samplingrange,

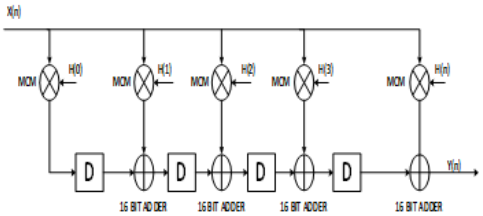

Figure 1: FIR Filter Design with MCM Multiplier

impulse response based filtering order and cut-off frequency. In this FIR filter design, will have number of adders, multipliers and delayed element is required to response filter output. An FIR filter is not computed any rounding errors in summing and multiplication. An FIR filter is inherently stable to produce output values and it can be no maximum value impulse response Nth order times, it can easily design and also easily configure sequence of linear phase coefficient, it will also applicable to detect the phase sensitive application such as crossover filter design, mastering, seismology and data communications. In this filter to meet the coefficient specification in certain things, which can be suitable with time domain and frequency domain. The

main disadvantages of FIR Filter design and more power consumption and large area size is required for multiplier, adders and delayed element in number of Nth order.

In the High performance FIR Filer architecture will have MCM Multiplication and normal adders will perform inherently pipelined and also produce the results on significant way with save computation results. In the FIR Filter design will take large area and also take the stringent order to meet frequency range with high performance. In the Fig.1 architecture will have to used MCM(Multiple constant multiplication), adders and delayed element, here the MCM multiplier will not identified the method of signed and unsigned operation, the multiplier will configure either signed or unsigned. In the FIR filter Nth order of the filter increases, a efficiency of FIR will increases, then the number of addition and multiplication required get increased. For the efficient realization of FIR filter i) Distributed Arithmetic (DA) and ii) Multiple Constant Multiplication (MCM) methods are used. In DA-design, to reduce the computation lookup tables are used for the storage of pre-computed results. In MCM method, the additions required for computation get reduce and it is more effective because it uses common sub-expression sharing [1]. This method of blocks is formed only in transpose form and it is suitable for large order filter implementation with fixed co-efficient.

In this proposed approach of this work, is to modified a MCM multiplier to approximate multiplier for improving the speed and energy efficiency. Approximate multiplier of arithmetic operations will performs different design of abstraction levels and also performed different technique to handled to reduced timing violation (e.g. voltage over scaling, or over clocking). In this paper we focus on proposing high speed and low power with low energy level of approximate multiplier using FIR filter design. The proposed approximate multiplier of ROBA (Rounding based approximate multiplier) will perform both signed and unsigned operation with three optimized architecture. The paper is contributions and it can be summarized as follows,

a) To modified a conventional multiplication and approach a new scheme of ROBA multiplication.

b) The approach of ROBA multiplier will describing the hardware structure of three module with scheme of sign and un-sign multiplication operation.

c) Implement this ROBA Multiplier to replace the MCM Multiplication in FIR Filter and shown the performance.

The rest of this paper is organized as follows, Section II discusses the Approximate Multiplier and three hardware structure of Implementation. Section III describe the structure and functionality of Brent Kang Adder Design. Section IV describe a FIR Filter design with ROBA Multiplier. Section V describe a Implementation Results and Reports. Finally, the conclusion is drawn in Section VI.

1. ROBA (ROUNDING BASED APPROXIMATE MULTIPLIER)

In a Approximate Multiplier design of ROBA Multiplier is to make of the ease of operations when the number are two to the power n (2^n). To elaborate the operation of this rounding based approximate Multiplier, first let us denote the rounded number of inputs of A and B by using approximation rounding method of Ar and Br respectively. The multiplication of A by B may be rewritten as,

$$A \times B = (Ar - A) \times (Br - B) + Ar \times B + Br \times A - Ar \times Br. \quad (1)$$

The key observation is that the multiplication of Ar x Br, Ar x B and Br x A may be implemented just by the shift operation. In this approach, the nearest value for A and B in the form of 2^n should be determined. When the value of A (or B) is equal to the $3 \times 2^{p-2}$ (where p is an arbitrary positive integer larger than one), it has two nearest values in the form of 2^n with equal absolute differences that are 2^p and 2^{p-1}. While both values lead to the same effect on the accuracy of the proposed multiplier, selecting the larger one (except for the case of p=2) leads to a smaller hardware implementation for determining the nearest rounded, and hence, it is consider in this paper. In originates from the fact that the numbers in the form of $3 \times 2^{p-2}$ are considered as do not care in both rounding up and down simplifying the process and smaller logic expressions may be achieved if they are used in the rounding up. The only exception is for three, which in this case, two is considered as its nearest value in proposed approximate multiplier.

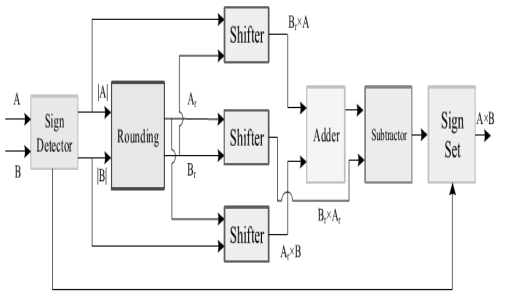

Figure 2: Block diagram for the proposed ROBA Multiplier

In the block diagram of Fig.2 where the inputs are represented to can give both sign and unsigned value. First a sign detector will the identified the inputs such as sign bit of MSB is '0' or '1', if the MSB bit is '0' the input data will consider as positive, if the MSB bit is '1' the input data will consider as negative, in the negative case the sign detector represented in two's complement format. Next the rounding block extracts the nearest value for each absolute value in the form of 2^n. To find the nearest value of input A, we use the following equation to determine each output bit of the rounding block:

$$Ar[n-1] = \overline{A[n-1]} \,.\, A[n-2] \,.\, A[n-3] \_\_\_\_\_ + A[n-1] \,.\, A[n-2]$$

$$Ar[n-2] = (\, \overline{A[n-2]} \,.\, A[n-3] \,.\, A[n-4] \_\_\_\_\_ + A[n-2] \,.\, A[n-3] \,) \,.\, A[n-1]$$

$$Ar[i] = (\, \overline{A[i]} \,.\, A[i-1] \,.\, A[i-2] + A[i] \,.\, \overline{A[i-1]} \,) \,.\, \overline{\sum^{n-1}_{i=i+1}} A[i]$$

$$Ar[3] = (\, \overline{A[3]} \,.\, A[2] \,.\, A[1] + A[3] \,.\, \overline{A[2]} \,) \,.\, \overline{\sum^{n-1}_{i=4}} A[i]$$
$$Ar[2] = A[2] \,.\, \overline{A[1]} \,.\, \overline{\sum^{n-1}_{i=3} A[i]}$$
$$Ar[1] = A[1] \,.\, \overline{\sum^{n-1}_{i=2} A[i]}$$
$$Ar[0] = A[0] \,.\, \overline{\sum^{n-1}_{i=1} A[i]} \quad (2)$$

In the Proposed equation, A[i] is one in two cases. In the first case, A[i] is one and all the bits on its left side are zero while A[i-1] is zero. In the second case, when A[i] and all is left side bits are zero, A[i-1] and A[i-2] are both one. Having determined the rounding values, using three barrel shifter blocks, the products Ar x Br, Ar x B, Br x A are calculated [2]. Hench, a single 2n-bit Brent kung adder is used to calculate the summation of Ar x B and Br x A. The output of this adder and the results of Ar x Br are the inputs of the Sub-tractor block whose output is the absolute value of the output of the proposed multiplier. Because Ar and Br are in the form of 2^n, the inputs of the sub-tractor may take our of the three inputs patterns shown in Table 1. Then configure the sign correction using Sign Set block and finally get the output of A x B.

Table 1: All Possible Cases for Ar x Br and Ar x B + Br x A values

Input 1 (Ar x B + Br x A)	Input 2 (Ar x Br)	Output
000…11..xxx	000…10..xxx	000…01..xxx
000…11..xxx	000…01..xxx	000…10..xxx
000…10..xxx	000…01..xxx	000…01..xxx

2. BRENT KUNG PARALLEL PREFIX ADDER DESIGN

In the Binary addition and basic arithmetic operation in all digital circuits and it became most essential in Arithmetic and logic unit and digital signal processing application. A research on present technology its continues on increasing the adder's delay performance. In many recent applications like mobile, laptops and telecommunications devices, to be increases a better performance in area and power to improved FPGA architecture its better than microprocessor and DSP's based solutions. The parallel prefix architecture of adders is common in high performance in signal processing application it will proved logarithmically proportional to the adder size. The parallel prefix adders essentially consists of three adder structure such as pre computation, prefix stage and final computation.

Pre computation:

In a parallel prefix adder a pre computation step, to generated and propagates the output based on following equations.

$$P_i = A_i \text{ xor } B_i$$
$$G_i = A_i \text{ and } B_i \quad (3)$$

The propagated carry equation are given as,

$$C_1 = G_0 + P_0 \, C_0$$
$$C_2 = G_1 + P_1 \, G_1 + P_1 \, P_0 \, C_0$$
$$C_3 = G_2 + P_2 \, G_1 + P_2 \, P_1 \, G_0 + P_2 \, P_1 \, P_0 \, C_0$$
$$C_4 = G_3 + P_3 \, G_2 + P_3 \, P_2 \, G_1 + P_3 \, P_2 \, P_1 \, G_0 + P_3 \, P_2 \, P_1 \, P_0 \, C_0$$
$$S(4)$$

Prefix stage:

In a parallel prefix adder design a prefix stage, will consist of two things generate and propagate signal its computes the each bits of inputs and output in prefix adder structure, this prefix stage will have two cells such as black cell (BC) its generates the structured pair in equation (4), the gray call (GC) generates only left signal,

$$G_{i:k} = G_{i:j} + P_{i:j} \cdot G_{j-1:k}$$
$$P_{i:k} = P_{i:j} \cdot P_{j-1:k} \quad (5)$$

More, basically, the equation (5) can be expressed using a symbol "0" denote by Brent and kung. Its function is exactly the same as that of a black cell i.e.

$$G_{i:k} = P_{i:k} = (G_{i:j} : P_{i:j}) 0 (G_{j-1:k} : P_{j-1:k}) \quad (6)$$

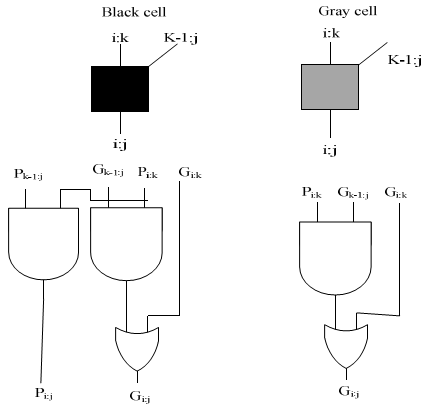

Figure 3: Black and Gray cell logic Definitions

The "0" operations will help make the rules of building prefix structures.

Final computation:

In the final computation, the sum and carry out are the final output.

$$S_i = P_i \cdot G_{i-1:-1}$$
$$C_{out} = G_{n:-1} \quad (7)$$

Where "-1" is the position of carry input. The generate and propagate signal can be grouped in different manner to get the same correct carry. Based on different ways of combination the generate and propagate signals, different prefix architecture can be created. Fig.3 Shows the definitions of cells that are used in prefix structure, including BC and GC [3].

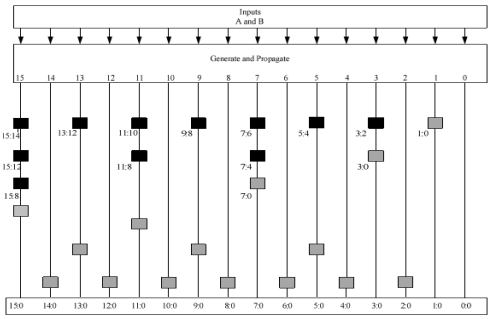

Figure 4: Brent Kung Adder design

3. PROPOSED FIR FILTER DESIGN WITH ROBA APPROXIMATE MULTIPLIER

A Multiplier is more important in today technology in the application of digital signal processing, image processing and cryptography application method, since this all applications is a most high priority in today technology such as 3G, LTE, Tele-communication, audio and video processing and so on. In this DSP application, the multiplier is the main priority to reduce the signal noise, fluctuation in all type of gadgets. In this method of Rounding based approximate multiplier is fully design based on approximate value with both signed and unsigned input and output operation method with brent kung adder. This method of approximate multiplier will simplified to some shift and add operations, and it will reduced the average errors at the price of increasing hardware complexity. In Fig.5 Shown the architecture of FIR Filter design with Rounded based approximate multiplier.

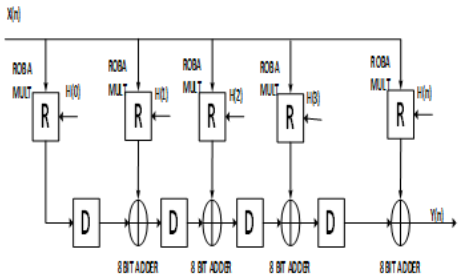

Figure 5: Proposed FIR Filter Design with ROBA Multiplier

An FIR filter is not required a feedback based inputs, which means, this filters is not computed any rounding

errors, in summing and multiplication. An FIR filter is inherently stable to produce output values and it can be no maximum value impulse response Nth order times, it can easily design and also easily configure sequence of linear phase coefficient, it will also applicable to detect the phase sensitive application such as crossover filter design, mastering, seismology and data communication. In this filter to meet the coefficient specification in certain things, which can be suitable with time domain and frequency domain. The main disadvantages of FIR filter design are more power consumption and large area size is required for multipliers, adders and delayed element in number of Nth order based TAP. In the High performance FIR filter architecture of Fig.1 will have MCM multiplication and normal adders it will perform inherently pipelined and also produced the result on significant way with save computation results. This MCM multiplier will not identified signed and unsigned operation of inputs, and not concentrate on carry operation inside of partial products addition. In the FIR filter design will take large area and also take the stringent order to meet frequency range with high performance.

The proposed architecture of Fig.5 will have to replaced the MCM multiplication to Rounding based approximate multiplication, in this paper we focus on proposing a high speed and low/energy yet approximate multiplier appropriate for error resilient in DSP applications such as voltage over-scaling, over clocking and so on. The proposed approximate multiplier, which is also area efficient, is constructed by modifying the conventional multiplication approach at the algorithm level assuming rounded input values. We call this rounding based approximate (ROBA) multiplier. The proposed FIR filter design approach is applicable to both signed and unsigned operations now the proposed thing to resolve the jitter noise, over clocking, frequency mismatching, cut-off frequency troubling and so on.

Hardware Implementation

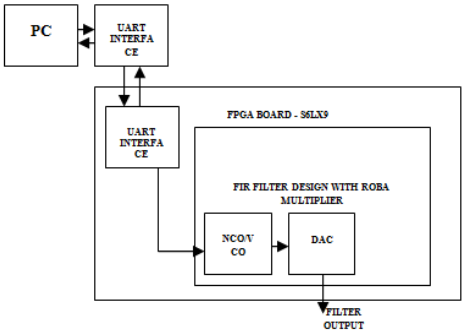

Figure 6: Hardware Implementation Block Diagram

In the Fig.6, the Input will provided through UART commnication regarding the input frequency changes for testing, such as the UART data will provide the Threshold value of 0, 1, 2, 3,… N, based upon this NCO modulator will provide the output frequency in variation. In this FIR Filter Design we configure a Low Pass Filter at Sampling frequency (fs) = 100MHz and Cut off frequency (fc) = 5MHz, Here the proposed module will test the input frequency range with help of NCO Modulator up to 1 - 10MHz. The input frequency will provided to FIR filter, and the output frequency will taken through DAC Interface, and test the DAC output using Oscilloscope. The Low pass filter will configure in FIR Filter using Filter Co-efficient it will generated from MATLAB Tool.

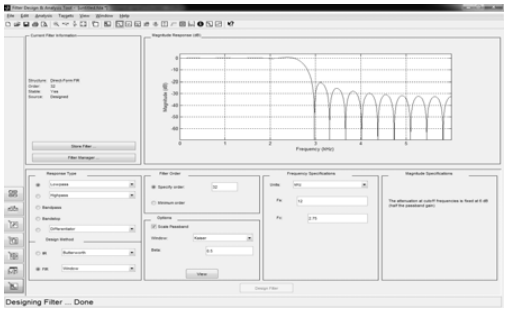

Figure 6: MATLAB Filter Generation

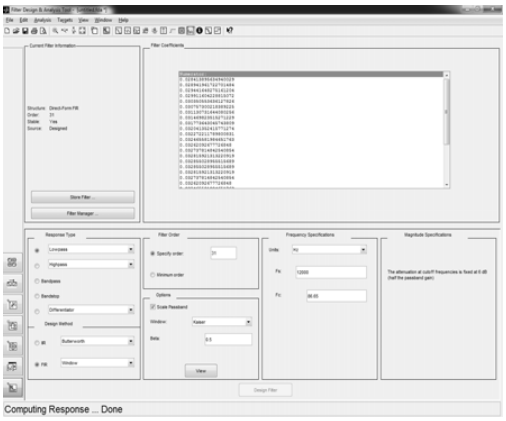

Figure 7: Coefficient generation for 5Mhz

4. IMPLEMENTATION RESULTS

In Table.2 will provide the Comparison of MCM and ROBA Multiplier will design at 8-Bit level, here our proposed ROBA Multiplier will take lowest power consumption compared to MCM Design.

Table 2: Comparison of MCM and ROBA Multiplier

	Existing System - MCM - Signed	Proposed System - ROBA - Signed / Unsigned
Number of Slice Registers	16	0
Number of Slice LUT	5	111
Number of Occupied Slice	9	45
Number of IOB	33	32
Total Power (mW)	113	14
Delay(ns)	3.593	41.726
Fanout effect	1.42	2.34

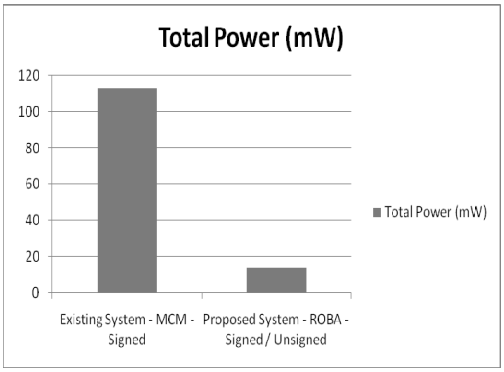

Figure 8: Power consumption of MCM and ROBA Multitier

In Table.3 will provide the Comparison of MCM and ROBA Multiplier using FIR Filter Design it will design at 8-Bit level and 16-Tap, here our proposed of ROBA Multiplier using FIR Filter Design will take lowest power consumption, Slice registers with compared to MCM Multiplier using FIR Filter Design.

Table 3 : Comparison of FIR Filter with MCM and ROBA Multiplier

	Existing System - 16TAP	Proposed System-16TAP
Number of Slice Registers	1446	751
Number of Slice LUT	618	2005
Number of Occupied Slice	314	721
Number of IOB	26	26
Total Power (mW)	114	14
Delay(ns)	2.362	17.980
Fanout effect	1.97	2.42

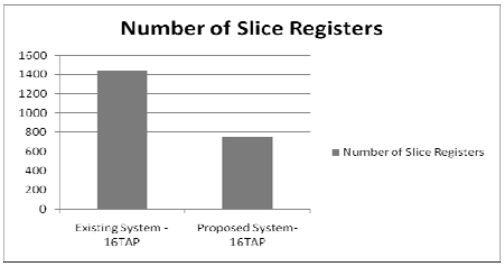

Figure 9 : Slice Register for FIR Filter with MCM and ROBA Multiplier

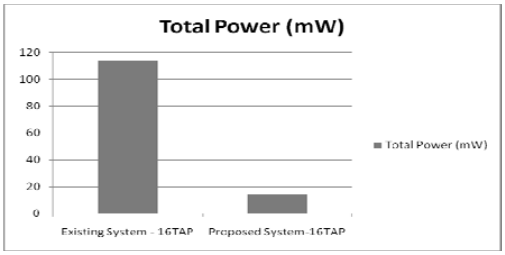

Figure 10: Power consumption for FIR Filter with MCM and ROBA Multitier

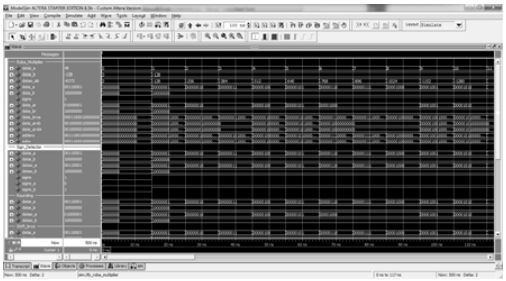

Figure 11: Simulation output of ROBA Multiplier

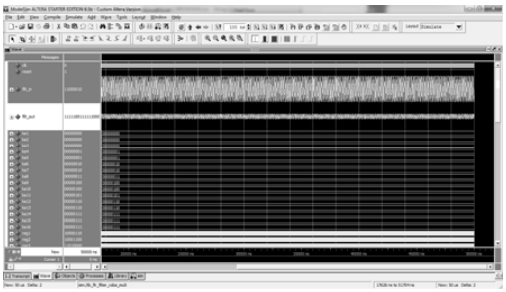

Figure 12: Simulation output of FIR Filter at fc=5Mhz, fs=100Mhz, Input frequency more than Cut-off freq.

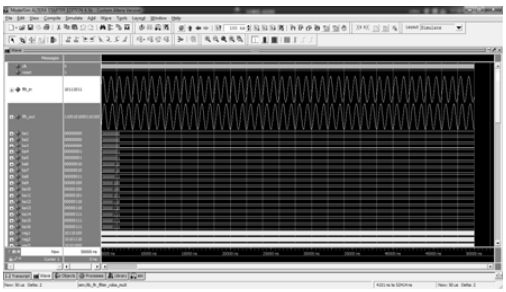

Figure 13: Simulation output of FIR Filter at fc=5Mhz, fs=100Mhz, Input frequency less than Cut-off freq.

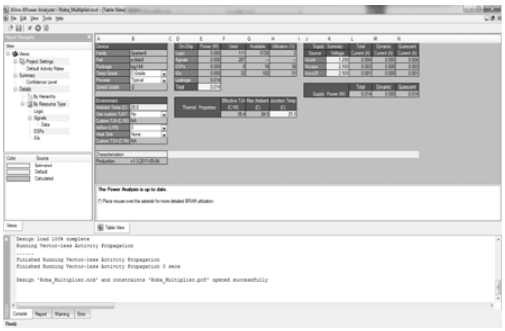

Figure 14: Power report for ROBA Multiplier

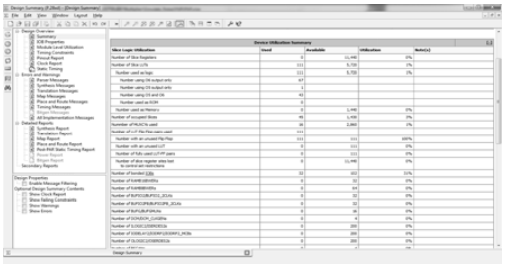

Figure 15: Area Report for ROBA Multiplier

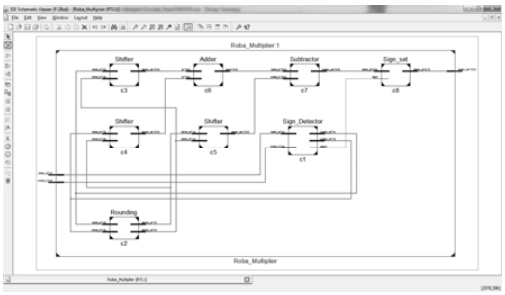

Figure 16: RTL Schematic for ROBA Multiplier

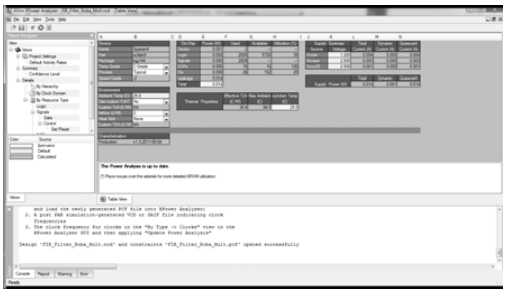

Figure 17: Power Report for FIR Filter Design

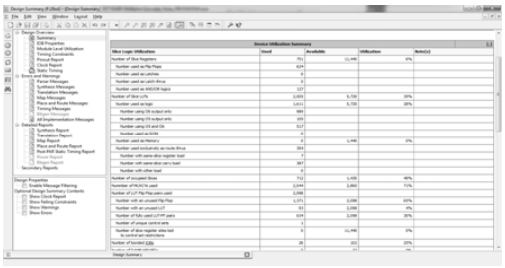

Figure 18: Area Report for FIR Filter Design

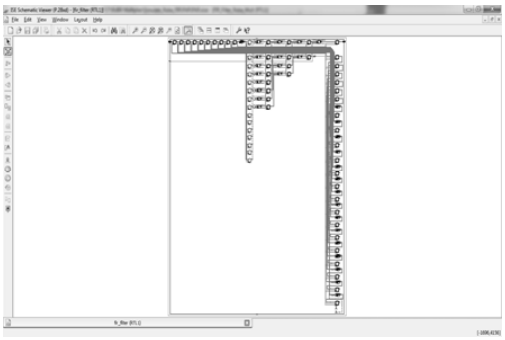

Figure 19: RTL Schematic of FIR Filter Design

5. CONCLUSION

In this paper, we have proposed on FIR Filter Design with Rounding Based Approximate Multiplier with Brent Kung Adder, and the performance will be proved area, power and delay and also successfully implemented the technology of signed and unsigned operation based multiplier in FIR Filter Design, and reduces the signal noise, fluctuation, over clocking and over scaling. In this method the Table.2 proved the comparison of MCM Multiplication and ROBA Multiplier, Table.3 will proved the comparison of FIR Filter with MCM and FIR Filter with ROBA Multiplier and finally the proposed architecture will designed in VHDL and synthesized in Xilinx FPGA S6LX9, and shown the comparison of Area, Power and Delay. Enhancement of this Project we can use this FIR filter design to integrate with DSP application, such as DWT, Mell Filter, Loop Filter, CIC Filter and so on.

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