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A NOVEL METHOD OF OBSTACLE AND SLEW AWARE 3-D GATED CLOCK TREE SYNTHESIS

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Abstract

In present VLSI technology power consumption in 3-D Clock tree synthesis is an important factor to be considered among other factors such as area and speed. In 3-D CTS the process of insertion of buffer, makes it below standard area and power consumption with the consideration of wirelength and clock-skew. In this paper, a new methodology of designing 3-D gated CTS is proposed which helps the designer to construct a required clock tree with low dynamic power consumption and minimize the clock skew. While constructing 3-D gated clock tree synthesis flip flop switching

activities and time constraint of signal has been considered.so it can reduce a power consumption of about 20% by cost effective way. formulating marketing strategies by both the existing and new retail outlets.

Keywords : Reduced power VLSI, Clock skew, Clock tree synthesis,

1. INTRODUCTION

In VLSI technology, the quality of clock network plays an essential role in synchronous chip. It has been a key aspects of design process which directly affects the performance of the chip.
The 3-D clock Tree Synthesis is an important element and problem in physical design which controls the speed of the whole circuit. It requires accurate timing analysis in order to control the clock slew among different parts of the clock tree. In clock tree synthesis, buffer insertion becomes unavoidable which reduces signal integrity and delay of the circuit. In clock tree synthesis, it requires separate buffer insertion by using specialized buffer algorithm. The clock buffer consumes the current at the clock edges. A large amount of current is generated around the clock edges, which leads to more power consumption buffer insertion along the routing path brings difficultly to maintain accurate delay. There have been several proposed works which have tried to reduce the power consumption around the clock edges. In this paper, a new methodology is approached to reduce the power consumption by using gated circuit instead of buffer to reduce power consumption.
The application of the gate insertion is an effective approach to reduce power. This principle leads to turn off the clock signal of the idle circuits.

2. CLOCK TREE:

Clock tree is an important terminology in the physical design process which takes place after placement. It is the heart of the physical design process. Each branch of clock tree can be represented by a distributed resistance-capacitance segment by buffer insertion. In the clock tree, there are n-nodes in which buffers are inserted in level by level manner. By constructing Clock tree using buffer delay clock skew/zero skew can be reduced.

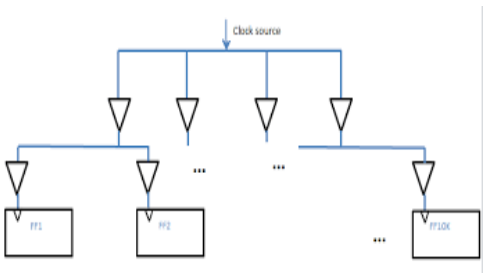

Fig 1: Clock tree

3. 3-D INTERCONNECT:

In electronics, 3-D IC is a chip in which two or more layers of active electronic components are integrated both vertically and horizontally into a single circuit.

By using 3-D technology in VLSI, it increases the functionality of the chip. It also increases the performance at low cost and with minimum power dissipation by reducing the chip area.

4. CLOCK GATING:

Clock gating is a popular technique which is used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to circuit to the clock tree.

The clock gating process saves significant die area and power. The clock gating technique can be implemented by using Register Transfer Level(RTL) Algorithm.

Clock gating can also be implemented in asynchronous circuits. In asynchronous circuits the clock gating is referred to as "Perfect Clock Gating". There is also automatic clock gating in which the hardware can be told to identify whether there is any work to do and turnoff a given clock if it is not needed to reduce power consumption.

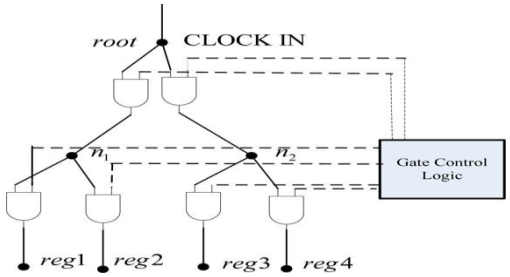

Fig 2: Clock gating technique

5. EXISTING METHODS

Different design factors are used to reduce the power consumption such as controlling the bound of TSV load capacitance and by adjusting the clock source location in the 3-D stack. By using these wirelength, skew can be reduced and produce more routing congestion and requires more buffer capacitance.[2]

In one of the most representative methods, Jingweri Lu[11] generated a clock tree by using gated logic instead of buffer. To construct a clock tree, two gated synthesizers are required such as Power Aware Clock Tree Synthesizer (PACTS) and Power-and slew aware Clock Tree Synthesizer (PSACTS). In this,

clock tree is constructed simultaneously by reducing skew and slew but requires more space during placement. Skew and delay can be reduced by the reliable buffer insertion by adjusting the wirelength and overcome the zero skew and provides the reliability disturbance.

The delay occurs based on the number of buffers and their location in the clock tree[12]. Construction of effective gated clock tree is based on the logical and physical information between the registers during placement by implementing the node merging and zero skew clock routing, so that gates are inserted in an accurate location based on the internal node information. The control gated logic signal is generated from the centralized gate controller [14].

An effective and efficient frame work to construct a clock tree with obstacle avoidance DME algorithm is used to reduce the skew and slew at the same time. Instead of buffer, loading capacitance is used to produce accurate result. It is proposed to handle the buffer, wirelength, slew obstacle and skew are reduced simultaneously. Different size of buffer are used, so that wire length can be reduced[13].

6. PROPOSED METHOD

The clock tree constructed using gated circuits is proposed instead of using buffer. Gated logic construction of clock tree is one of the tremendous technology to reduce dynamic power consumption in the circuits. Constructing clock tree using buffer dissipates large amount of power due to switching of clock to the circuits which are idle. But in this proposed method of introducing gated clock tree only small amount of power is consumed by shutting off the clock signal routing path which are idle. In this the cell block is constant and the registers are flexible.

7. MICROWIND

Microwind is an integrated EDA tool software that allows the designer to simulate and integrates the circuits at the physical level. It provides schematic entry, pattern based stimulation, spice stimulation, layout stimulation, cross sectional and 3 D viewer. The microwind library package contains common digital and analog ICs to view and simulate and reduces the design complexities.

8. RESULT ANALYSIS:

The simulated output using MICROWIND software is given below:

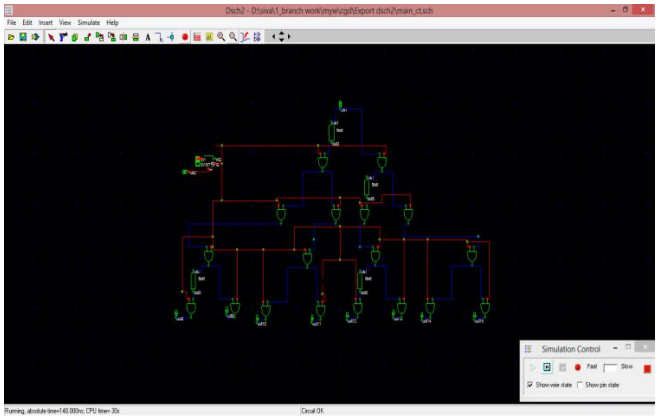

Fig 3: 3-D gated clock tree

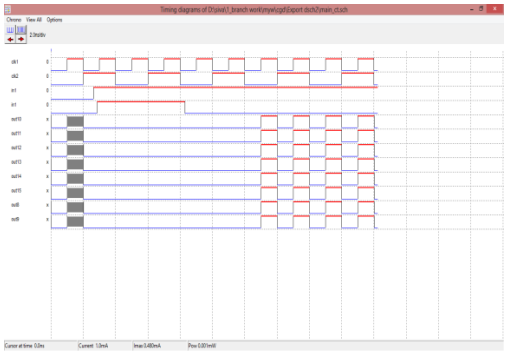

Fig 4: output of 3-d gated clock tree

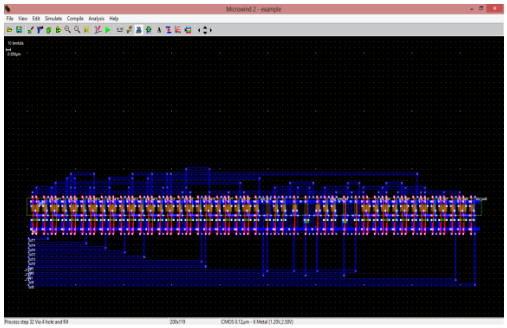

Fig: Layout design

9. CONCLUSION

In this paper a new method of constructing a clock tree using gated circuits in 3- dimension is proposed which mainly includes the register clustering during placement process. Construction of clock tree is done simultaneously by inserting gated circuits. Compared to previous gated works the proposed algorithm reduces the power consumption by about 20%. We can implement this methodology in application based system which consumes more power.

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