Design & Analysis of 2-phase Op-Amp for LDO Application

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Abstract

This paper presents 2-phase operational -Amplifier that can be cast-off for LDO application that provides a very high value of PSRR, CMRR, Phase margin and Gain. The proposed design was implemented in UMC 180nm technology. The topology of the design circuit entails of a differential pair tracked up through a CSA and common drain configuration which is used for loading purposes. The proposed design is used to obtain a high PSRR value of 98.277dB which is used for LDO solicitations. Simulation is done exhausting software Cadence, Virtuoso, Spectre and Assura under 1.8V to obtain Gain of 61dB and Phase margin of 60.045deg at unity bandwidth of 43.892MHz with power dissipation less than 0.214mW along with CMRR of 62.309dB. A full custom IC layout design occupies the area of about 20,000 square micrometers.

Keywords: Op-Amp, LDO, UMC, CMRR, PSRR

1. Introduction

Operational amplifier is an essential portion of analog and mixed signal system. The design of high-enactment op-amp has continuously been one of the hotspots of AIC analog integrated circuit design as its concert straight affects the comprehensive performance of circuits and system [6]. So, suitable proposal of Op-Amp is required for an actual application. It is required to achieve high value of PSRR for LDO application so that ripples at the input side can be rejected.

LDO device topology typically entails of input voltage, band gap reference, Op-Amp, filtering resistor and PMOS pass transistor as shown in Fig 1. LDO is a device which gives a constant output voltage irrespective of the supply voltage.

A complete analysis of 2-stage Op-Amp is depicted in this paper along with complete layout which leads to high value of PSRR and Gain. Design of conventional Op-Amp with source and its improved design with biasing resistor presented in Section II. In Section III, complete analyses of Op-Amp with design equations are given which will result in obtaining the transistor dimensions. Further, simulation results of Op-Amp and LDO are shown in Section IV. Graphical illustration of Gain and Phase margin, PSRR, CMRR, Slew rate are shown for Op-Amp along with Line and load regulations for LDO. The results obtained are compared with results from previous papers in tabular column. Section V concludes the paper with future work on the proposed circuit design.
II. 2-STAGE OPERATIONAL AMPLIFIER

Op-Amp is significant fragment of countless AMS analog and mixed signal circuits. Today use of mixed mode combined circuits increases. Analog circuits particularly Op-Amp in CMOS technology are problematic to design due to challenging tasks like counting various incompatible benchmarks and a wide diversity of design factors[3].

It is customary to know that the ideal current source in the schematic design of a 2-stage Op-Amp is difficult to implement in layout design. So the current source $I_{bias}$ is replaced with a Biasing Resistor, which is explained below.

<table>
<thead>
<tr>
<th>TABLE I: Design specifications</th>
<th>Expected Results</th>
<th>Obtained Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>1.8V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Technology</td>
<td>UMC 180nm</td>
<td>UMC 180nm</td>
</tr>
<tr>
<td>Gain</td>
<td>60 dB</td>
<td>61 dB</td>
</tr>
<tr>
<td>Phase margin</td>
<td>&gt;60dB</td>
<td>60.05dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>&gt;80dB</td>
<td>98.277dB</td>
</tr>
<tr>
<td>CMRR</td>
<td>&gt;60dB</td>
<td>62.309dB</td>
</tr>
<tr>
<td>Slew rate</td>
<td>0.5 V/μs</td>
<td>0.71 V/μs</td>
</tr>
</tbody>
</table>

Procedure to replace $I_{bias}$:

First perform DC analysis for the Op-Amp as explained in the

![Fig. 3: Replacing $I_{bias}$ with Resistor](image-url)
next section. Note down the node voltages across the current source I_	ext{bias} and do calculations as follows. Fig. 4.4 shows the voltage across I_	ext{bias} is 1 V. Now the aim is to get the R values should be such that voltage appearing across resistor is same as that across I_	ext{bias}. i.e. V_R = 1V Therefore the value of is given by 

$$R = \frac{V}{I} = \frac{1}{(30\mu)} = 34 \, \text{K}\Omega$$

![Fig. 4: Proposed transistor version of Op-Amp](image)

In the Fig 4, the biasing resistor is introduced which replaces the current source.

## III. DESIGN EQUATIONS (COMPLETE ANALYSIS)

### A. Calculation of Kn and Kp Values From Cadence technology file

Given, \( \varepsilon_o = 8.854 \times 10^{-12} \text{ F/m} \), \( \varepsilon_{ox} = 3.9 \); 

Capacitance per unit area \( C_{ox} = \frac{(\varepsilon_o \cdot \varepsilon_{ox})}{(t_{ox})} \)

Then, \( K_n = n \cdot C_{ox} = (0.0492)(8.22) = 404.4 \text{ uA/V}^2 \)

\( K_p = p \cdot C_{ox} = (0.0117)(8.22) = 96.17 \text{ uA/V}^2 \)

### TABLE II: Spice parameters from UMC 180nm CMOS technology

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{th} ) (V)</td>
<td>0.386</td>
<td>0.478</td>
</tr>
<tr>
<td>( \mu \cdot \text{m}^2/\text{V} \cdot \text{sec} )</td>
<td>0.0492</td>
<td>0.01172</td>
</tr>
<tr>
<td>( t_{ox} ) (nm)</td>
<td>4.2</td>
<td>4.2</td>
</tr>
</tbody>
</table>

### B. Design Procedure

**Step-1:** Determining Coupling Capacitance

Let \( L = 360\text{nm} \)

For PM=60deg:

\( C_C \geq 0.22 \, C_L \)

\( C_C \geq 0.22 \, \text{(3 pF)} \)

\( C_C \geq 0.66 \, \text{pF} \)

**Step-2:** Determining \( I_{SD} \) from Slew Rate (SR)

Let \( C_C = 0.1 \, \text{pF} = 100 \, \text{fF} \)

For PM=60:

\( SR = ISD/CC \)

\( ISD = SR \times CC \)

\( I_{SD} = 0.5\mu A \times 100\text{fF} \)

\( ISD = 5\mu A \)

\( V_{SD} = V_{SG} - V_{TP} = VDD - VBIAS - VTP \)

\( V_{DD} = 1.8 \, -1.25 \, -0.43 = 0.12 \text{ V} \)

\( I_{SD1} = I_{SD2} = \frac{I_{SD}}{2} = \frac{5\mu A}{2} = 2.5\mu A \)

**Step-3:** Determining \( \left( \frac{W}{L} \right)_t \) from WGB and ICMR+ specification

From \( WGB \) specification.
\[ W_{GB} = \frac{2n_m}{C_C} = \frac{1}{C_C} \sqrt{\frac{2K_p (W/L)}{I_{SD1}}} \]

\[ g_m = C_C \times W_{GB} \]

\[ g_m = (0.1p) \times (2\pi \times 50M) = 31.4\mu h o \]

\[ (\frac{W}{L})_1 = \frac{2^3 (31.4)^3}{2(50)p(2.5p)} = 1.8 \]

The +ve ICMR description,

\[ V_{G1(max)} = VDD - VSD5(SAT) - VSG1 \]

\[ V_{G1} = VDD - VSD5(SAT) - VGI(max) \]

From gate bias, \( V_{BIAS}, \ V_{SD5} \) can be derived.

\[ V_{SG1} = 1.8 - 0.12 - 1 = 0.68V \]

\[ V_{SD1(SAT)} = |V_{TP}| = 0.68 - | - 0.43 | = 0.25 \]

\[ (\frac{W}{L})_1 = \frac{2^4 I_{D61}}{K_p \times V_{DD}(SAT)} = \frac{2\times 2.5p}{55p\times (0.25)^2} = 3 \]

To mollify both conditions, we need select large (W/L) ratio.

For equivalent and equilibrium, we also select

\[ (\frac{W}{L})_1 = (\frac{W}{L})_2 = 3 \]

Step 4: Determining \((\frac{W}{L})_3\) from ICMR - specification

\[ (\frac{W}{L})_3 = \frac{2^4 I_{DD3}}{K_p \times V_{G21(min)} - V_{SS}} = \frac{2\times 2.5p}{34p\times (1.5 - (-1.8))^2} = 3 \]

Now we approximate \((\frac{W}{L})_4 = (\frac{W}{L})_1 = 1 \)

Step 5: Determining \((\frac{W}{L})_6\) from PM specification

\[ PM = 90 - \tan^{-1}(W_{GB}Z) - \tan^{-1}(W_{GB}P_2) \]

\[ W_{GB} = \frac{2n_m}{C_C} ; \ Z = \frac{2n_m}{C_C} ; \ P_2 = \frac{2n_m}{C_1+C_2} ; \ Z < P_2 \]

\[ C_C > C_1+C_2 \]

A suspicious appraisal of PM is obtained by presumptuous

\[ Z = P_2; \ 	ext{that is,} \]

\[ PM < 90 - 2\tan^{-1}\left(\frac{2n_m(C_C)}{2n_m(C_C)}\right) = 90 - \tan^{-1}\left(\frac{2n_m}{2n_m}\right) \]

\[ \tan^{-1}\left(\frac{2n_m}{2n_m}\right) < \frac{90-PM}{2} \]

\[ g_m > \left(\frac{2n_m\pi}{PM}\right) \]

To achieve PM >60deg

\[ g_m > \left(\frac{2n_m(31.4\mu h o)}{2}\right) = 117.186\mu h o = 120\mu h o \]

from step 5:

\[ VSD6(SAT) = VSD6(SAT) = 0.12V \]

\[ (\frac{W}{L})_6 = \frac{g_m}{K_p \times V_{DDB}(SAT)} = \frac{(31.4\mu)(0.12)}{2(34p)(2.898)} = 2.898 \]

The current through M6 is given by

\[ I_{DS6} = \frac{(g_m)^3}{2K_n(W/L)_6} = \frac{(31.4\mu)^3}{2(34p)(2.898)} = 7.2\mu A \]

For balanced condition, the current through \( M_6 \) must be properly ratio-ed with the current through \( M_6 \), i.e.,

\[ I_{DS6} = \frac{V_{DS6}}{(W/L)_6} = \frac{3.1\mu}{(W/L)_6} = 7.2\mu A \]

Step 6: Determining \((\frac{W}{L})_7\) from the balancing condition

we know that \( I_{DD5} = I_{DD6} \)

\[ (\frac{W}{L})_7 = \frac{I_{DD5}}{(W/L)_7} = 18.17 \]

Step 7: Determining \((\frac{W}{L})_8\) from the output resistance specification

\[ R_O = \frac{1}{g_m} = \sqrt{\frac{2K_p}{I_{DD8}}(\frac{1}{2})} \]

Solving for \( (\frac{W}{L})_8 \) assuming \( I_{DD8} = 30\mu A \)

\[ (\frac{W}{L})_8 = \frac{2K_p}{2(55p)(1.56)^2(30\mu)} = 34.68 \]

Step 8: Determining \((\frac{W}{L})_9\) of current mirror

Let \( I_{DD9} = 30\mu A \).

Choose \( V_{G26} = |V_{TP}| + 0.12 = 0.55 \) to guarantee its operation in saturation.

Now,

\[ (\frac{W}{L})_9 = \frac{2I_{DD9}}{K_p(V_{G26} - |V_{TP}|)^2} = \frac{30\mu}{(55p)(0.55 - | - 0.43|)^2} = 75.75 \]

As

\[ I_{SD9} = I_{SD10} = 30\mu A, (\frac{W}{L})_9 = (\frac{W}{L})_10 = 75.75 \]
This completes the design part of the op-amp. The results are tabulated as follows:

**TABLE III: Design Summary of Op-Amp**

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Ratio</th>
<th>W(micro)</th>
<th>L(micro)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>3</td>
<td>1.08</td>
<td>0.36</td>
</tr>
<tr>
<td>M2</td>
<td>3</td>
<td>1.08</td>
<td>0.36</td>
</tr>
<tr>
<td>M3</td>
<td>1</td>
<td>0.36</td>
<td>0.36</td>
</tr>
<tr>
<td>M4</td>
<td>1</td>
<td>0.36</td>
<td>0.36</td>
</tr>
<tr>
<td>M5</td>
<td>12.62</td>
<td>4.5432</td>
<td>0.36</td>
</tr>
<tr>
<td>M6</td>
<td>3</td>
<td>1.08</td>
<td>0.36</td>
</tr>
<tr>
<td>M7</td>
<td>18.17</td>
<td>6.5412</td>
<td>0.36</td>
</tr>
<tr>
<td>M8</td>
<td>34.68</td>
<td>12.4848</td>
<td>0.36</td>
</tr>
<tr>
<td>M9</td>
<td>75.75</td>
<td>27.27</td>
<td>0.36</td>
</tr>
<tr>
<td>M10</td>
<td>75.75</td>
<td>27.27</td>
<td>0.36</td>
</tr>
</tbody>
</table>

**IV. Simulation**

Simulation is done using Cadence, Virtuoso, Spectre and Assura to obtain Gain of 61dB and Phase margin of 60.045deg at unity bandwidth of 43.892MHz with power dissipation less than 0.214mW along with CMRR of 62.309dB. The AC analysis plot is shown in Fig 5. The corresponding figure indicating the PSRR value of 98.277dB is as shown in the Figure 6. High value of PSRR is advantageous because it will reject the ripples from the input terminal of Low dropout voltage regulator.

![AC Analysis](Fig 5)

![PSRR Measurement](Fig 6)

![CMRR Measurement](Fig 7)

![Stability Analysis](Fig 8)

![Power dissipation](Fig 9)
The corresponding AC graph indicating the CMRR value of 62.309 dB is shown in the Figure 7. The Stability analysis which is used to find out the value of Phase Margin and Frequency (Hz) of the opamp is shown in Fig 8. The Opamp can be tested should as low as possible (Power Consumed) and the results obtained for the same clearly seen in Fig 9.

Low drop out voltage regulator-Line and Load regulation

Line Regulation is the capability to maintain regulated output voltage irrespective of changes in the input line voltage. The obtained graph for Line regulation is given in Fig. 10.

![Fig 10 Line regulation of the LDO circuit](image1)

![Fig. 11: Load regulation of LDO circuit](image2)

Load Regulation is the capability to uphold regulated output voltage irrespective of changes in the output load. The obtained graph for Load regulation is given in Fig. 11. The comparison of various results of proposed design with previous papers is done and tabulated as shown below

| Table IV: Comparison of prior art
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tech(um)</td>
<td>0.13</td>
<td>0.35</td>
<td>0.18</td>
<td>0.18</td>
<td>0.65</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>3.3</td>
<td>2.5</td>
<td>-</td>
<td>2</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>85.93</td>
<td>78</td>
<td>80</td>
<td>59.19</td>
<td>96.64</td>
</tr>
<tr>
<td>PM (deg)</td>
<td>-</td>
<td>63.9</td>
<td>65</td>
<td>63.53</td>
<td>-</td>
</tr>
<tr>
<td>CMRR(dB)</td>
<td>61</td>
<td>-</td>
<td>-</td>
<td>67.08</td>
<td>-</td>
</tr>
<tr>
<td>PSRR(dB)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>63.84</td>
<td>-</td>
</tr>
</tbody>
</table>

| This Work       |        |        |        | 0.18   | 1.8    |
|                 |        |        |        | 62     | 60.045 |
|                 |        |        |        | 62.809 | 98.277 |
V. CONCLUSION AND FUTURE SCOPE

The operational amplifier presented in this paper is designed using 180nm UMC technology to obtain a gain of 61.58dB and extremely high PSRR value of 99.277dB working with 1.8V supply. Phase margin of 61.045deg at unity bandwidth of 43.892MHz with power dissipation less than 0.214mW and CMRR of 62.309dB is recorded. Hence this Op-Amp is used in order to design an LDO and the results obtained are clearly indicative of its use for LDO Application.

Folded Cascode Op-Amp with Class AB amplifier combined at its load can be used to advance the stability of the amplifier. This biasing is called trans linear or Monticelli biasing. Furthermore, gain boosting techniques can be employed for high gain applications.

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References

Journals


Books


Conferences


Authors

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