

Elimination of Dead time in inverter for industrial applications

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Abstract—Analysis of a dead-time elimination method is presented in this paper for voltage source inverters. In conventional H-bridge voltage source inverter, different techniques are employed to provide gate pulse to MOSFET which purposely introduced dead time to avoid shoot through faults. This paper analysis a new technique using a modification of the existing conventional H-bridge circuit to eliminate the dead time in voltage source inverter. In the conventional circuit there is a problem of output distortion, harmonic effect and fundamental rms output voltage is reduced. Even though harmonics can be filtered, dead time is introduced in the conventional circuit to avoid shoot through fault. In this new method all the above problems are reduced and have the quality load voltage significantly improved. The proposed technique has been verified and the results are obtained from simulations using PSpice.

Index Terms—Dead-time, harmonic, phase-leg, Pulse width modulation (PWM) control.

INTRODUCTION

To avoid shootthrough in voltage source inverter (VSI), dead time, a small interval during which both upper and lower switches in a phase leg are off is introduced into the standard pulse width modulation (PWM) control of VSIs. However, such a blanking time can cause problems such as output waveform distortion and fundamental voltage loss in VSIs, especially when the output voltage is low.[1-7]

To overcome dead time effects, most solution focus on dead-time compensation by introducing complicated PWM compensators and expensive current detection hardware.

A new method, [1] based on angle domain repetitive control, to reduce the distortion in PWM inverter output waveforms caused by the dead time and the zero-current crossing. Repetitive control is not useful when the period of

input/disturbance signal varies with time. In reference [2] presents a new switching strategy for PWM power converters. It can reduce the discontinuous phenomenon of the current, which occurs in the conventional dead time minimization method, at the changing instant of the current polarity. A dead-time minimization algorithm was also discussed in [3] to improve the inverter output performance. In reference [4], a disturbance observer was used to evaluate the compensating voltage on-line, the inputs to the observer being the output current and the back electromotive force (EMF) of the motor supplied from the inverter. This method, however, requires adequate knowledge of the load parameters and the operating point. In reference [5] uses compensation term whose magnitude depends on the rms output current; this improves the accuracy of compensation with respect to the fundamental, but the problem of harmonic distortion remains unresolved. In reference [6] the compensation is implemented by adjusting the switching frequency to avoid unfeasible pulse widths of the gating signals, as well as to minimize the total harmonic distortion of the inverter output voltage. Higher switching frequencies improve waveform quality by raising the order of principle harmonics; but low-frequency sub harmonics may persist in the output voltage. Detailed analysis of different technique are discussed in paper [7] to [10]

For general applications, automatically eliminating dead-time by gate drive technology is a desired and complete solution. Gate drives with intelligent functions are in high demand due to the emerging technology of power electronics building blocks (PEBB) and intelligent power modules (IPM) because smart functions can improve power devices' modularity, flexibility and reliability

In this paper, analysis of effective dead time elimination is proposed. This method is based on decomposing of a generic phase-leg into two basic switching cells, which are configured with a controllable switch in series with an uncontrollable diode. [11-17] Therefore, dead-time is not needed. The principle of the proposed method to eliminate dead-time effect is explained in detail. Simulation and experimental results are provided to demonstrate the validity and features of the proposed method.

I. DEAD- TIMEEFFECTS

Fig. 1 shows the ideal switching patterns and gate drive signals containing the dead time for an inverter leg. The S_p and S_n are the ideal switching pattern of the positive device and the negative device of U phase, respectively. To avoid the so-called shoot-through, the actual gate drive signals must be delayed by the dead time. [18-21] The gate drive signals containing the dead time are denoted as S_{pd} and S_{nd} . Since the gate drive signals are shifted from the centre of the sampling interval by the unwanted dead time, the generated phase voltage is also shifted as much as the delay time is. Although the produced voltage pulses resulting from each of the gate drive signals during the sampling intervals are not much affected, the resultant voltage during an entire cycle is significantly reduced due to the dead time. In addition, those cumulated delays distort the output waveform of the inverter.

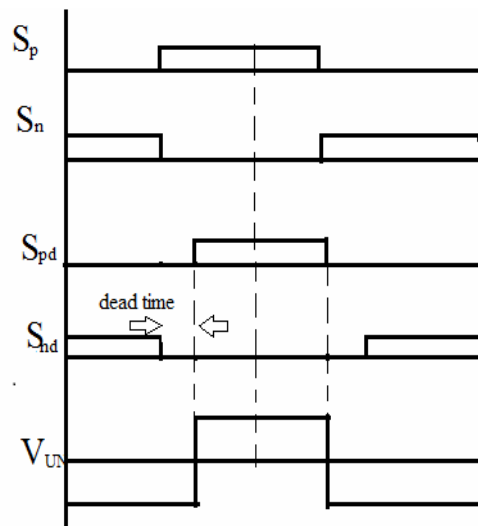


Fig 1 Gate drive signals of PWM inverters

The full bridge circuit feeding an inductive (RL) load is shown in fig 2(a).

Fig.2 (b) shows the dead time effects on output voltage in a voltage source inverter.

The output voltage, as shown in fig 2(b) has harmonic components in addition to the fundamental component.[22-24] The harmonic components can be filtered out by including filter on the output side. The filter may not be necessary especially when the load is inductive such as an induction motor.

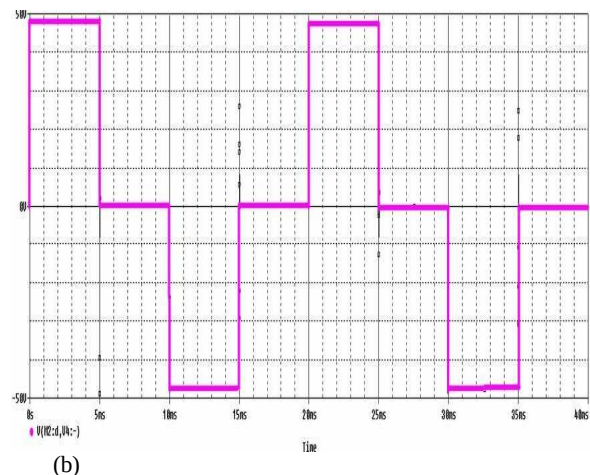
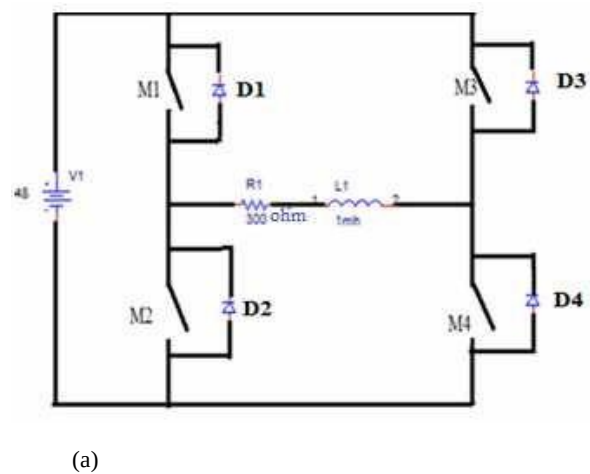


Fig 2 Effect of dead-time on output voltage

When a switch is gated on but the current is in the opposite direction, the freewheeling diode placed in anti- parallel with the switch will provide the path for the current. Note that there are two intervals during which the output voltage is zero is shown in fig 2(b).

With conventional gate pulse control, the output voltage distortion is inevitable since dead-time must be added to avoid a shoot-through circuit in [18-21] VSIs. In next section, the analysis of a dead-time elimination method is proposed. This method is based on decomposing of a generic phase-leg into two basic switching cells, which are configured with a controllable switch in series with an uncontrollable diode. As a result, the output distortion can be effectively reduced.

II. ANALYSIS OF PROPOSED METHOD

A. Experimental Circuit

The power circuit diagram for the dual bridge converter with no dead time operation is as shown in fig 3.

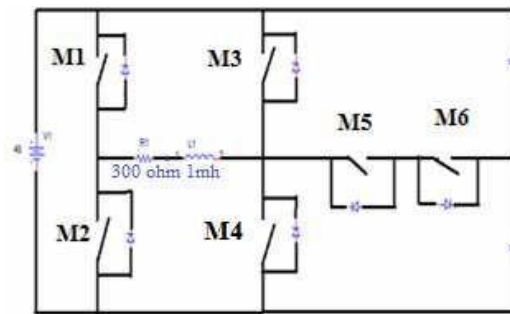


Fig 3. Power Circuit of dual bridge converter

B. Modes of operation:

Mode 1:

In this mode of operation the switches M_1 and M_4 of the full bridge and the switch M_5 of the half bridge are in the conducting state and the corresponding [17] current flow is as shown in the fig 4(a).

Mode 2:

In this mode of operation switch M_1 of the full bridge and the switches M_5 and M_6 of the half bridge are in the conduction state and the current flow in the circuit is as shown in the fig 4(b).

Mode 3:

In this mode of operation the switches M_2 , M_6 and M_3 of the full bridge are in the conduction state and the current flow in the circuit is as shown in the fig 4(c). [25]

Mode 4:

In this mode of operation the switch M_2 of the full bridge inverter circuit and the switches M_5 and M_6 of the half bridge are in the conduction state and the current flow direction in the circuit is shown in the fig 4(d).

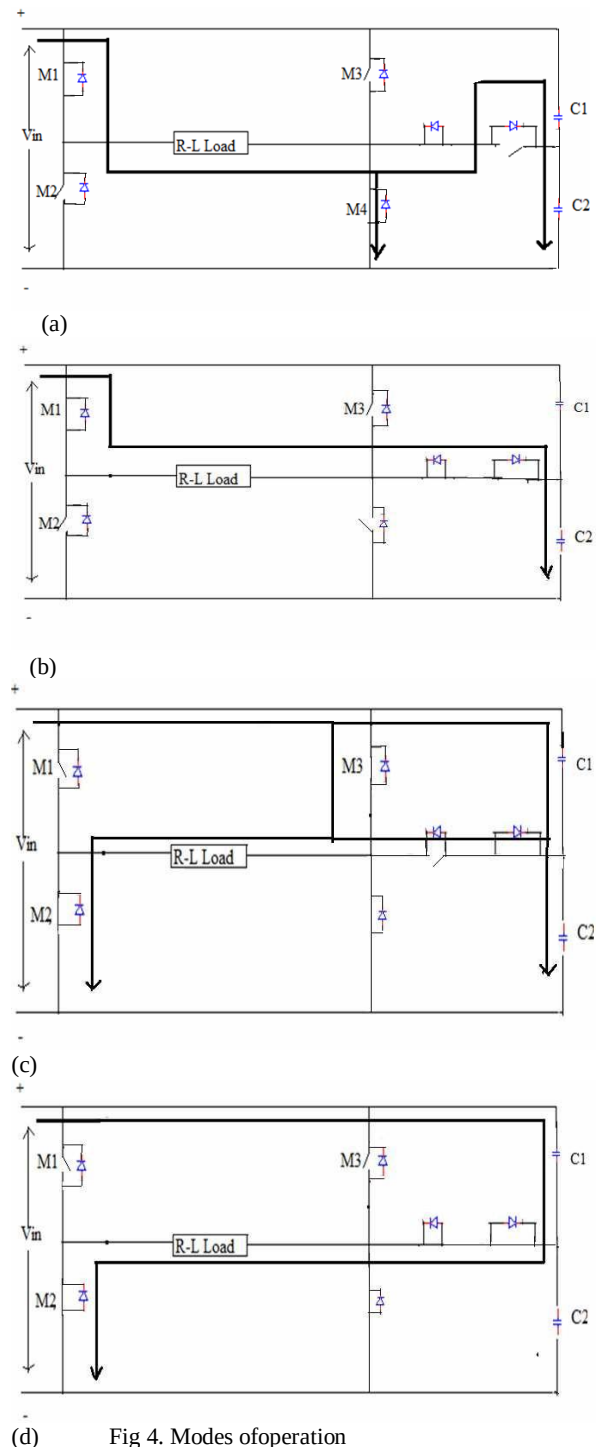


Fig 4. Modes of operation

III. SIMULATION RESULTS

Simulation of power electronic converters can be done, either by circuit oriented simulator PSPICE or by mathematical model based equation solvers using high level languages.

To validate the proposed dead-time elimination method, an H-bridge inverter shown in Fig. 5 has been simulated using PSPICE software. [28] The load consists of a 1 mH inductor and a 100 ohm resistor. The dc bus voltage is set to 48 V and the inverter is controlled by voltage pulse.

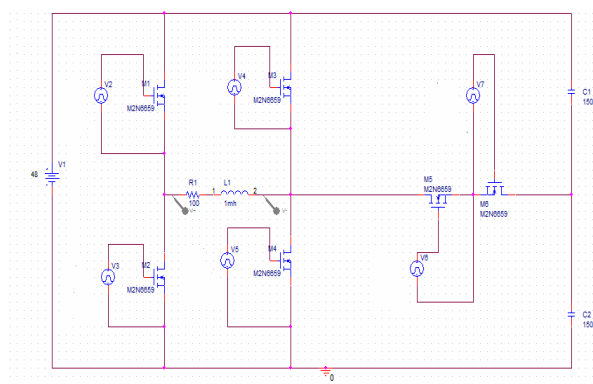


Fig 5. Simulation circuit of proposed model

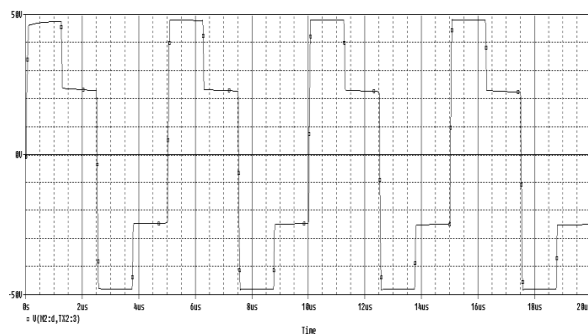
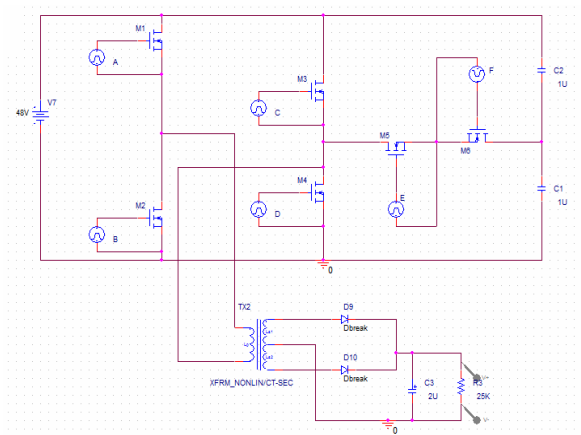
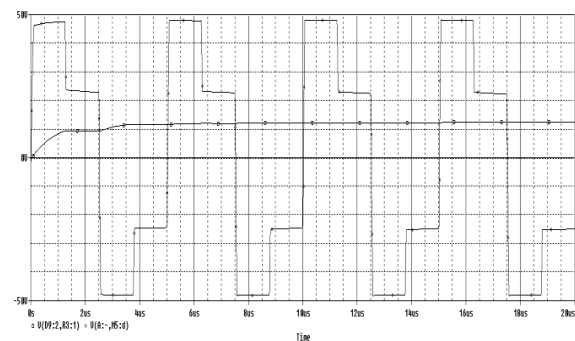


Fig 6. Output voltage without dead time
Compare with an output voltage shown in fig. 6 with fig. 2(b) dead time is eliminated in the above fig. 6. For application oriented the output of ac voltage is rectified and given to a resistive load. The waveform is shown in the fig.7[40-45]



(a)



(b)

Fig 7 inverter for d.c application

III. CONCLUSION

In this paper a novel method was proposed to eliminate dead time for voltage source inverters. Compared to standard PWM control including dead-time and conventional dead-time compensation methods, the proposed method has the following advantages which make it an attractive option for VSI applications.

- Significantly reduces the output distortion and regains the output RMS value;
- Reduces gate drive power and minimizes switching loss;
- Reduces gate drive power and minimizes switching loss since switches are only active for half of each fundamental cycle;
- Reliable since a delay is automatically inserted if the output current is zero or near zero;
- Simple circuit and low cost;
- Simple control logic and flexible implementation.

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