Bridgeless SEPIC PFC Converter – A Review

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Abstract—There is a need to improve the power quality of the grid as well as the power factor implied on the grid due to the nonlinear loads connected to it. A new single phase bridgeless AC/DC power factor correction (PFC) topology to improve the power factor as well as the total harmonic distortion (THD) of the utility grid is proposed in this research. By eliminating the input bridge in conventional PFC converters, the control circuit is simplified; the total harmonics distortion THD and power factor PF are improved. The controller operates in multi loop fashion as the outer control loop calculates the reference current through innovative filtering and signal processing. Inner current loop generates PWM switching signals through the PI controller. Analytical derivation of the proposed converter is presented in detail. Performance of the proposed PFC topology is verified for prototype using PSIM circuit simulations. The experimental system is developed, and the experimental results agree with simulation results.

INTRODUCTION

The request for developing power quality of the AC system has drawn excessive interest during the recent years. The increased usage of power electronic devices, such as variable speed drives, uncontrolled rectifiers and other switching devices, affects the power quality of the utility grid significantly. Standards similar to International Electro technical Commission (IEC) 61000-3-2 restrict the harmonics generated by these equipments [1-7]. To reduce harmonics in energy transmission lines, the research on active power factor correction (PFC) techniques has taken on an accelerated path.

Typical PFC converter topologies are boost [6,7], buck-boost [8], buck [9-11] and SEPIC [12-17]. The boost PFC converter is often used in practical applications, as the input current can be conveniently formed into a sinusoidal waveform to obtain unity power factor. However, the boost PFC converter has a restricted capability since the DC output

The input current of the buck PFC converter has dead zones along the cycle, which requires extensive passive filtering to improve the power factor. There is a tradeoff between output voltage choice and power factor. To solve this problem, SEPIC or Cuk converters were proposed. A conventional SEPIC converter can supply a high power factor in wide range of voltage conditions [12-13]. The output voltage could be reduced or increased without the need of inversion with the SEPIC converters[14].

This paper presents a new topology for single phase bridgeless AC/DC PFC converters that reduces the THD and improves the PF of the operation. Proposed SEPIC converter combines the bridge and DC-DC stages into one stage. Section 2 analyses operation of the proposed SEPIC PFC converter. In Section 3, component selection and control circuit design are presented. The simulation results of the conventional and proposed SEPIC converter are presented in Section 4. Summary and future work is provided in Section 5.

Here, load draws current from the output capacitor C0. During this situation, the voltage of the input inductor will be same as the rectified AC voltage Vac. Besides input capacitor’s voltage and output inductor’s voltage are equal to Vac during this mode of operation. In the second mode, the switch turns off, diode

2. PFC CONVERTER

The conventional SEPIC PFC converter is shown in Figure 1 [15]. The operation of the circuit can be separated in to two modes concerning the position of the switches. When the switch Q1 is switched on, output diode D is reverse biased [18-24]. input inductor L1 starts to charge, output inductor L2 and AC input capacitor C1 creates resonant circuit.

increases linearly until the diode current extinguishes. When D turns off, output side is disengaged from
the input side, the current through the inductors freewheel at the input side. Working modes for proposed SEPIC PFC converter is provided in Figure 3.

3. PRINCIPLE OF OPERATION
Since the proposed SEPIC converter circuit comprises of two symmetrical structures as shown in Fig. 3, the circuit is investigated for the positive half cycle structure. Suggesting that the circuit working in a positive half cycle of a switching period $T_s$ can be divided into three working modes, as shown in Fig. 3(a)-(c) and it can be defined as follows.

Mode 1: In this mode, $Q_1$, $Q_3$ and $Q_4$ switches are turned on, as shown in Fig. 3(a). In this mode, the input inductor currents increase and output inductor current decreases linearly at a rate proportional to the input voltage $V_{ac}$. The rate of increase of the input inductor currents and the rate of decrease of output inductor current are given [30-34].
DESIGN OF CONVERTER

The standard design equations for the main components of the AC/DC SEPIC PFC converter are provided in [15-17]. The proposed converter is designed for 25 Vrms, 60 Hz AC input voltage to generate at 10 V DC. The input transient input voltage, input current, output voltage, output current and output power for the conventional bridgeless SEPIC PFC converter. Figure 6 presents the input voltage and input current for the conventional bridgeless SEPIC PFC converter. Figure 7 presents the transient input voltage, input current, output voltage, output current and output power for the proposed bridgeless SEPIC PFC converter. Figure 8 presents the input voltage and input current for the proposed bridgeless SEPIC PFC converter. It can be seen from the Figure 8 that input current is in phase with input voltage and is sinusoidal with low THD and high PF values. Output voltage is obtained at about 10V, with a 120 Hz low frequency ripple[25-29].

The multi loop control is proposed for the converter, outer voltage controller generating the reference current to regulate the DC voltage and the inner PI controller generating the gating signals as shown in Figure 4. The high frequency switching of the converter produces switching ripples on the DC voltage. Thus the measured DC voltage is processed through a band stop filter to eliminate the noise on the measurements[35-41].

4. SIMULATION RESULTS

The proposed single phase bridgeless SEPIC topology is simulated by PSIM with the parameters based on the design provided in Section 4. Figure 5 presents the transient input voltage, input current, output voltage, output power for the conventional bridgeless SEPIC PFC converter. Figure 7 presents the transient signals for proposed SEPIC PFC converter.
The simulation results of the PF and THD values for a conventional SEPIC PFC converter, proposed bridgeless SEPIC PFC converter are provided in Table 1. The proposed converter is able to reduce the THD 3.23% from 8.93% and improve the power factor to 0.998. The proposed topology provides much better THD and PF compared to conventional one.

**TABLE 1. COMPARISON OF BRIDGELESS SEPIC PFCs**

<table>
<thead>
<tr>
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<th>THD (%)</th>
<th>PF</th>
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<tr>
<td>Conventional SEPIC PFC</td>
<td>8.93%</td>
<td>99.3%</td>
</tr>
<tr>
<td>Proposed bridgeless SEPIC PFC</td>
<td>3.23%</td>
<td>99.8%</td>
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5. EXPERIMENTAL RESULTS

The experimental circuit of the proposed converter is developed for the design provided in Section 4. The experimental setup is provided in Figure 9.

Input inductors L1, L3 and output inductor L2 are made with toroidal core from Micro metals T300-60D (turn=205, wire=23AWG) and T184-2 (turn=65, wire=18AWG) respectively. IRF840PBF (500V, 8A) for switches and LXA06T600 (fast recovery, 600V, 6A, Vf=2.94V) for diodes are selected. The control circuit is implemented using a TMS320F28335 digital signal processing DSP [42-45].

The experimental results of input voltage, input current and output voltage for conventional SEPIC PFC are shown in Fig. 10 and 11. For the input voltage of 25 Vrms, output voltage of 10 Vrms, and the input current of 140 mA, the THD is measured to be 5.722%, with a power factor of 0.995.

The experimental results of input voltage, input current and output voltage for the proposed SEPIC PFC are shown in Fig. 12 and 13. For the input voltage of 25 Vrms, output voltage of 10 Vrms, and the input current of 136 mA, the THD is measured to be 2.837%, with a power factor of 0.998. The output voltage ripple is obtained 0.15 V at 10 Vdc as it is shown in Fig. 13. The phase of the input current is similar to the input voltage and the obtained PF is near unity.

Fig. 8. The input voltage and current for proposed SEPIC PFC

Fig. 9. The experimental prototype for proposed SEPIC converter
The proposed converter is able to reduce the THD by 2.83% from 5.72% and improve the power factor to 0.998. It is found that the proposed bridgeless SEPIC PFC converter topology provides much better performance than conventional SEPIC PFC converter. The topology is implemented on a converter operating from 25 V AC input to generate 10 V DC. The proposed converter topology is very good for single phase bridgeless SEPIC PFC solution for lower power equipments.

Fig. 11. Experimental result for conventional SEPIC PFC. \( V_s = 25 \text{ Vrms}, I_s = 140 \text{ mA} \) with \( \text{THD} = 5.72\% \), \( V_{dc} = 10 \text{ Vrms} \) and \( \text{PF} = 0.995 \).

Fig. 13. Experimental result for proposed SEPIC PFC. \( V_s = 25 \text{ Vrms}, I_s = 136 \text{ mA} \) with \( \text{THD} = 2.83\% \), \( V_{dc} = 10 \text{ Vrms} \) and \( \text{PF} = 0.998 \).

Fig. 12. Experimental result for proposed SEPIC PFC. (a) Input voltage and (b) input current.

SIMULATION RESULTS

OUTPUT WAVEFORM
6. CONCLUSION
In this paper, a new single phase bridgeless SEPIC PFC converter topology is proposed, analyzed and verified with the simulations. In order to improve the power factor as well as the THD of the utility grid, the full bridge diode in input is removed. Through simulation and experimental studies the performance of the proposed SEPIC converter topology are

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