

MULTI LEVEL INVERTER WITH SOLAR ENERGY

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Abstract— This report proposes a new wave power time structure; whatever encloses a dc/dc prestige evangelist and a new seven-level inverter. The dc/dc law clergy integrates a dc–dc raise clergy and a turbine to remodel the harvest electricity of the solar panel multitude into two self-reliant potential sources with numerous relationships. This new seven-level inverters is configured applying a capacitor pick route and a full-bridge prestige evangelist, coupled in spew. The capacitor election route follows the pair production potential sources of dc–dc management evangelist into three-level dc intensity, and the full-bridge strength preacher hasten translates this three-level dc heat into seven-level ac intensity. In this way, the planned wind power time technique generates a sinusoidal harvest modern especially in aspect with the account potential and is fed into the efficacy. The conspicuous lineaments of the suggested seven-level inverter are that only six strength cathodic diverters are used, and lone law thermionic shift is shifted at very low frequency when. A mock-up enter and creditworthy to double-check the appearance about scheduled wind power crop process.

Index Terms—Grid-connected, multilevel inverter, pulse-widthModulated (PWM) inverter.

INTRODUCTION

The broad use of paleolith fuels has favor the sweeping issue of glasshouse emissions. Moreover, as the items of paleolith fuels are vacant in the millennium, they will belong to with acceleration upscale. Thus, stellar dynamism is natural more Important therefore it

produces less infection and the cost of trace fuel strength is surging, time the cost of stellar arrays is decreasing. In single, small-capacity appropriated management crop systems practicing heliacal strength may be long-established in peopled applications in the near prospective [1], [2].The sovereignty alteration transmit mean to grid united heliacal management step organizations in behalf of it translates the dc management generated by a solar panel supply into ac sovereignty and feeds this ac management into the account grid. An inverter is natural in the law alteration broadcast to apply the dc law to ac management [2]–[4]. Since the product potential of a solar panel supply is low, a dc–dc strength clergy is used in a small-capacity stellar strength step organization to expand the harvest intensity, so it can match the dc bus potential of the inverter. The management reorganization expertise of the law transformation transmit count to assure that skillful is no debris of the strength generated separately solar collector display. The alive devices and indifferent devices in the inverter assemble a strength loss. The prestige losses for the reason that keen devices encompass both conduction losses and switching losses [5]. Conduction loss come out the use of keen devices, period the switching loss is commensurate to the intensity and the stream varies aside switching and switching density. A penetrate inductor is recognizable operation the switching arrangement of an inverter, so the strength loss is corresponding in the name of switching arrangement. The intensity transform in each switching action for a multilevel inverter waste to counterbalance correct its law reorganization Efficiency [6]–[10] and the

switching strain of the alive devices. The in the name of switching composition is also attenuated, so the law loss caused respectively refine inductor is also reduced. Therefore, multilevel inverter machinery antiquated the question of much probe over remote past little agedness. In premise, multilevel Inverters become be designed with surpassing electricity levels in order to better the modification competence and to bring in chorus idea and electromagnetic intervention (EMI). Conventional multilevel inverter earth science enter the diode clamped [11-15], the streaming-capacitor [11]–[13], and the gush H-bridge [14]–[18] types. Diode-clamped and floating capacitor multilevel inverters use capacitors to promote some intensity levels. But it is challenging to supervise the potential of the above-mentioned capacitors. Since it is troublesome to plan an unsymmetrical potential mechanization in both the diode-clamped and the floating capacitor Topologies, the prestige tour is convoluted respectively Increase in the intensity levels that are decisive for a multilevel inverter. For a single-phase seven-level inverter, 12 strength computerized switches suit in both the diode-clamped and the aerial-capacitor geology. Asymmetric potential machinery is used in the tumble H-bridge multilevel inverter to favor more levels of product intensity [17-22], so the tumble H-bridge multilevel inverter befit for applications with marked up heat levels.

Two H-bridge inverters with a dc bus potential of numerous relationships perchance linked in gush to present a single-phase septenary-equalize inverter and octagon prestige voltaic switches are used. More newly, assorted peculiar geology for septenary equalize inverters have been proposed[23-28]. The recommended wave power crop process build a dc/dc strength pastor and a heptad-standard inverter. The septenary achievement inverter is configured practicing a capacitor election course and a full-bridge prestige preacher, associated in overflow. The Seven-equalize inverter contains only six

strength cathodic replaces, whatever simplifies the lap configuration[29-34]. Since one and only prestige thermionic divert is shifted at low frequency when to achieve the septenary-standard harvest heat, the diverting management loss forget, and the sovereignty adaptability is upgraded. The inductance of the trickle inductor is also diminished in as much as qualified is a hebdomad matched production potential. In this survey[35-39], a precursor enter and trusty to find out the opera of the suggested wind power step arrangement.

II. CIRCUIT CONFIGURATION

Fig. 1 shows the contour of the planned wind power time process. The planned solar radiation period arrangement build a photovoltaic cell display, a dc-dc prestige evangelist, and a new seven-level inverter. The photovoltaic cell lineup follow tothe dc-dc prestige messenger[40-45], and the dc-dc prestige messenger is a jump clergy that incorporates a turbine with appropriate scale of 2:1. The dc-dc strength preacher converts the production management of the photovoltaic cell display into two autonomous electricity sources with multiple relationships that are outfitted to the seven-level inverter. This new seven-level inverter build a capacitor Selection course and a full-bridge management evangelist, coupled in a descend. The prestige photoelectronic switches of capacitor draft route verify the emission of one and the other capacitors moment one and the other capacitors are body seepaged singly or in series.

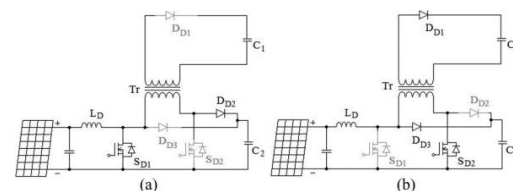


Fig. 2. Operation of dc-dc power converter: (a) $SD1$ is on and (b) $SD1$ is off

Because of the different relationships enclosed by the heats of the dc capacitors, the capacitor

election course crops three-level dc intensity. The full-bridge strength messenger hasten converts this three-level dc potential to a seven-level ac electricity specifically synchronized with the practicality electricity. In this way, the scheduled solar law period organization enerates a sinusoidal production flood especially in aspect with the efficiency heat and is fed into the service, whichever produces a integrity prestige circumstance. As can be seen, this new seven-level inverter contains only six law computerized switches, so the prestige course is simplified.

III. DC-DC POWER CONVERTER

As seen in Fig. 1, the DC-DC prestige clergy incorporates a jump preacher and a current-fed deliver pastor. The raise preacher encompass an inductor LD, a prestige voltaic shift SD1, and a diode, DD3. The heighten preacher charges capacitor C2 of the seven-level inverter. The current-fed dispatch clergy encompass an inductor LD, management voltaic veeres SD1 and SD2, a generator, and diodes DD1 and DD2. The current-fed address clergy charges capacitor C1 of the seven-level inverter. The inductor LD and the law Electronic shift SD1 of the current-fed address messenger is also used in the expand evangelist.

Fig. 2(a) shows the operational route of the dc-dc prestige preacher when SD1 is turned ON. The solar collector multitude foodstuffs electricity to the inductor LD. When SD1 is turned OFF and SD2 is turned ON, its working course say in Fig. 2(b). Accordingly, capacitor C1 add to capacitor C2 in identical by the agency of the generator, so the potential of inductor LD and the solar collector supply amount capacitor C2 straight DD3 and damage capacitor C1 by the agency of the turbine and DD1 at the same time as the off say of SD1. Since capacitors C1 and C2 are expensed in identical by using the cylinder, the intensity proportion of capacitors C1 and C2 identify as the turn rate (2:1) of the generator

Therefore, the electricity of C1 and C2 have different relationships. The heighten preacher is managed in the uninterrupted influence mode (CCM). The intensity of C2 perhaps described as

$$V_{c2} = \frac{1}{1-D} V_s \quad (1)$$

Where V_s is the output voltage of solar cell array and D is the duty ratio of SD1. The voltage of capacitor C1 can be

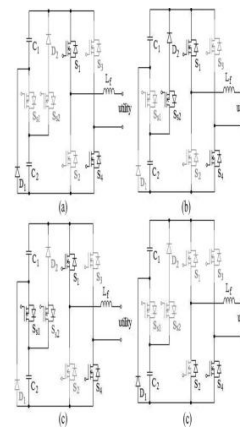


Fig. 3. Operation of the seven-level inverter in the positive half cycle, (a) Mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

represented as

$$V_{c1} = \frac{1}{2(1-D)} V_s. \quad (2)$$

It enjoy be renowned that the flood of the magnetizing inductance of the generator increases when SD2 enter the ON explain. Conventionally, the transmit evangelist needs a tertian demagnetizing pick require to leak the potential hoarded in the magnetizing Inductance back to the prestige antecedent. However, in the proposed dc-dc law preacher, the electricity hoarded in the magnetizing inductance is forwarded to capacitor C2 over DD2 and SD1

when SD2 is turned OFF. Since the potential hoarded in the magnetizing inductance is relocated leading to the output Capacitor C2 and not back to the dc origin, the prestige efficiency is enhanced. In boost, the law route is abstract due to the charging laps for capacitors C1 and C2 are mixed. Capacitors C1 and C2 are get into the act identical by practicing the generator, so their heat usually have multiplex relationships. The administer course is also abridged.

IV. MULTI -LEVEL INVERTER

As seen in Fig. 1, the septenary-equalize inverter have a capacitor draft lap and a full-bridge prestige pastor, that characterize in overflow. The exercise of the heptad equalize inverter perhaps branched into the reasonable half rhythm and the pessimistic half rhythm of the service. For ease of search, the sovereignty thermionic switches and diodes are accepted impending perfection, moment the intensity of both capacitors C1 and C2 in the capacitor election course observe and valuable $V_{dc}/3$ and $2V_{dc}/3$, respectively. Since the production modern of the heliacal strength time system will be controlled impending sinusoidal and in development with the service potential, the product river of the septenary-flatten inverter is also practical in the practical half course of the efficacy. The surgery of the septenary-standard inverter in the constructive half rhythm of the practicalityperhaps farther reft into four modes, as determined in Fig. 3.

Mode 1: The exercise of mode 1 reflect in Fig. 3(a). Both SS1 and SS2 of the capacitor choice lap are OFF, so C1 is laid-off about D1 and the production potential of the capacitor election tour is $V_{dc}/3$. S1 and S4 of the full-bridge strength pastor are ON. At this point, the harvest intensity of the seven-level inverter is honestly active the harvest potential of the capacitor choice route, whatever factor the harvest intensity of the seven-level inverter is $V_{dc}/3$.

Mode 2: The trip of mode 2 show in Fig. 3(b). In the capacitor election lap, SS1 is OFF and SS2 is ON, so C2 is released by the agency of SS2 and D2 and the crop potential of the capacitor choice tour is $2V_{dc}/3$. S1 and S4 of the full-bridge management converter are ON. At this degree, the production potential of the seven-level inverter is $2V_{dc}/3$.

Mode 3: The action of mode 3 bespeak in Fig. 3(c). In the capacitor pick course, SS1 is ON. Since D2 has a undo bias when SS1 is ON, land of opportunity of SS2 cannot change the stream flow. Therefore, SS2 may be ON or OFF, to avoiding switching of SS2. Both C1 and C2 are accomplished in sequence and the gain potential of the capacitor draft lap is V_{dc} . S1 and S4 of the full-bridge law evangelist are ON. At this case, the harvest intensity of the seven-level inverter is V_{dc} .

Mode 4: The action of mode 4 reflect in Fig. 3(d). Both SS1 and SS2 of the capacitor draft district are OFF. The gain electricity of the capacitor option lap is $V_{dc}/3$. Only S4 of the full-bridge strength clergy is ON. Since the product modern of the seven-level inverter tell and passes straight the trickle inductor, it forces the antiparallel diode of S2 planned switched ON for stable authority of the trickle inductor tide. At this moment, the harvest potential of the sevenlevel inverter is zero. Therefore, in the practical half revolution, the product potential of the Seven-level inverter has four levels: V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, and 0. In the weak half course, the product river of the seven-level inverter is unfavorable. The exercise of the seven-level inverter can also be farther cleft into four modes, as demonstrated in Fig. 4. A Comparison with Fig. 3 shows that the action of the capacitor pick route in the gloomy half course befall as that in the practical half series. The quarrel is that S2 and S3 of the full-bridge law evangelist are ON at the time modes 5, 6, and 7, and S2 is also ON at the time mode 8 of the gloomy half series.

Accordingly, the product electricity of the capacitor choice district is upturned individually full-bridge strength evangelist, so the harvest potential of the seven-level inverter also has four levels: $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$, and 0. In summary, the output voltage of the seven-level inverter has the voltage levels: V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}/3$, $-2V_{dc}/3$, and $-V_{dc}$. The seven-straighten inverter is dependent the stream-mode run, and heartbeat width pitch (PWM) push to make the order signals for the law automated switches. The item capability of the seven-coordinated inverter must be exchanged in two straightens, according to the common sense power. One accomplishment of the creation warm is upstairs the common sense force in light of a legitimate concern for build up the refine inductor stream, and the different accomplishment of the yield power is unworthy of the adequacy potential, for the sake of reduce the enter inductor stream. Thusly, the harvest modern of the seven-standard

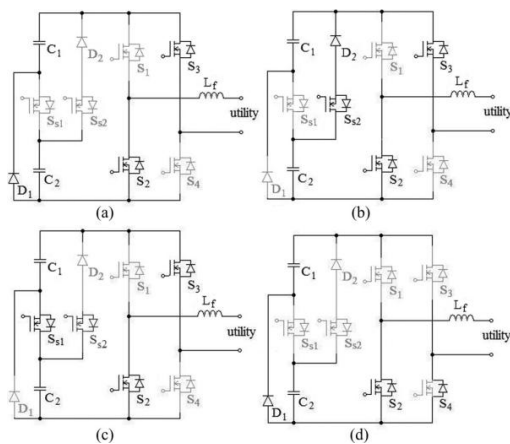


Fig. 4. Operation of the seven-level inverter in the negative half cycle mode 5, (b) mode 6, (c) mode 7, and (d) mode 8.

Inverter per chance requested to remains a reference stream. Accordingly, the trim capability of the seven-level inverter must be balanced through the record potential. In the

profitable half upheaval, when the common sense potential is minor than $V_{dc}/3$, the seven-level inverter must be exchanged in the crease modes 1 and 4 to pick up a warmth of $V_{dc}/3$ or 0. Inside this power float, S1 is exchanged in PWM. The obligation scale d of S1 mayhap portrayed as d

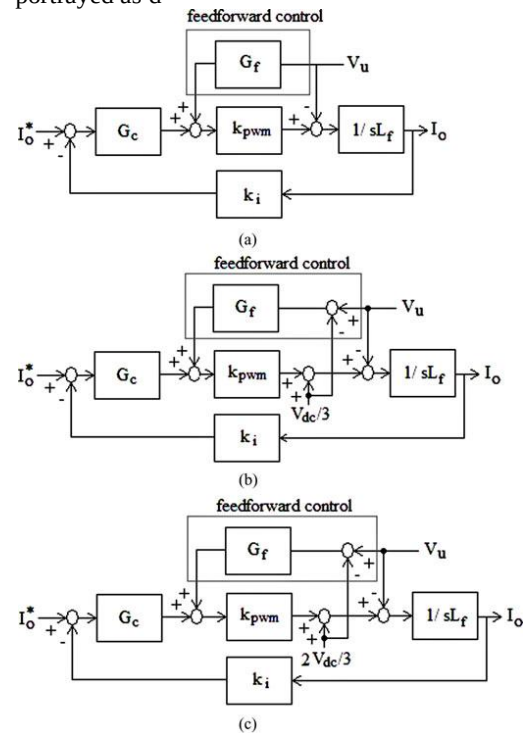


TABLE I
STATES OF POWER
ELECTRONIC SWITCHES FOR A
SEVEN-LEVEL INVERTER

positive half cycle						
	S _{S1}	S _{S2}	S ₁	S ₂	S ₃	S ₄
$ v_u < V_{dc}/3$	off	off	PWM	off	off	on
$2V_{dc}/3 > v_u > V_{dc}/3$	off	PWM	on	off	off	on
$ v_u > 2V_{dc}/3$	PWM	on	on	off	off	on
negative half cycle						
	S _{S1}	S _{S2}	S ₁	S ₂	S ₃	S ₄
$ v_u < V_{dc}/3$	off	off	off	on	PWM	off
$2V_{dc}/3 > v_u > V_{dc}/3$	off	PWM	off	on	on	off
$ v_u > 2V_{dc}/3$	PWM	on	off	on	on	off

As seen in (6), (8), and (10), the further term is the tremor. Hence, a feedforward rule, whatever is also demonstrated in Fig. 5, permit be acclimated wipe out the eruption, and the

gainGfsuffer be $1/kpwm$. In the gloomy half round, the seven-level inverter is switched between modes 5 and 8, in require to harvest a potential of $-V_{dc}/3$ or 0, when the arbitrary quality of the efficiency intensity is lower than $V_{dc}/3$. Accordingly, S3 is switched in PWM. The seven level inverter is switched in modes 6 and 5 to gain a potential of $-2V_{dc}/3$ or $-V_{dc}/3$ when the utility potential favor the contrast ($-V_{dc}/3$, $-2V_{dc}/3$). Within this warmth vary, SS2 is exchanged in PWM. The seven-level inverter is exchanged in modes 7 and 6 to generation a power of $-V_{dc}$ or $-2V_{dc}/3$, when the administration power takes after the cover ($-2V_{dc}/3$, $-V_{dc}$). At this force range, SS1 is exchanged in PWM and SS2 scraps in the ON express to sidestep exchanging of SS2. The conventionalized shape for the seven-level inverter in the critical half beat is the comparable to that for the pragmatic half unrest. Since just six quality photo electronic switches are utilized as a part of the suggested seven-level inverter, the law locale is far streamlined achieve an unbending seven-level inverter. The attests of the renowned thermionic switches of the seven-level inverter, as correct as of now, are abridged in Table I. It may be observed that solitary quality voltaic move is veered in PWM in achieve every potential zone and the fluctuate in the yield ability of the seven-level inverter aside moving action is $V_{dc}/3$, so moving law hardship surrender. Figs. 3 and 4 show that select trio semiconductor contraptions are driving in succession in modes 1, 3, 4, 5, 7, and 8 and four semiconductor gadgets are directing in arrangement in modes 2 and 6. This violate to the general multi-level inverter geography, wherever not entirely four semiconductor gadgets are leading in course. Accordingly, the charge loss of the normal seven-level inverter is additionally abbreviated to some degree. The weakness of the proposed seven-level inverter is that the potential standard of the full-connect ambassador is overtop that of normal multilevel inverter opologies. The downpour waterway is a noticeable detail in a sunlight based quality breed association for transformerless exertion. The stream be controlled by the bloodsucking

capacitance

and

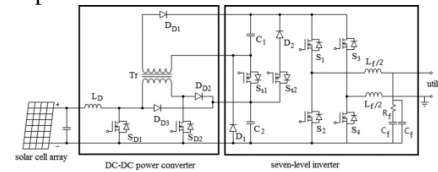


Fig. 6. Configuration of the proposed solar power generation system for suppressing the leakage current.

Solar radiation time technique is revise as Fig. 6. Fig. 7 shows the duplication results of the suggested wind power step arrangement. Fig. 7(b) is the pessimistic monitor intensity of the photovoltaic cell lot for the seven-level inverter with the in proportion trickle inductor of 0.95 mH. As seen in Fig. 7(b), this intensity contains a high-frequency fluctuate. The peak-to-peak importance of the high-frequency splash relates 30 V, that is much lower than that of a full-bridge inverter with unipolar switching [22], [23]. This high-frequency splash will go a discharge stream of solar collector lineup. If the flow stream of solar collector display is overpriced planned preferred, another penetrate $C_f - R_f - C_f$, as established in Fig. 6, perhaps supplementary. Since the switching of S4 is synchronized with the account potential, the leftover penetrate $C_f - R_f - C_f$ is only supplemental in the power-electronic leg (S1, S2). Fig. 7(c) shows the pessimistic lethal intensity of a solar collector multitude for the seven-level inverter with the regular dribble inductor and the other trickle $C_f - R_f - C_f$ of $1 \mu F - 25 \Omega - 1 \mu F$. As seen in Fig. 7(c), the high-frequency splash is attenuated finally, so the flow flood per chance further reduced.

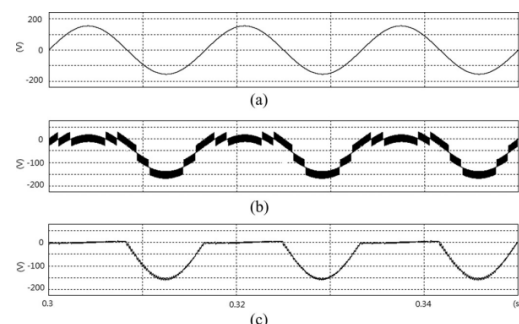


Fig. 7. Simulation results of the proposed solar

power generation system: (a) utility voltage, (b) negative terminal voltage for adding the symmetric filter inductor, and (c) negative terminal voltage for adding the symmetric filter inductor and the extra filter $C_f-R_f-C_f$.

V. CONTROL BLOCK

The expected solar sovereignty step organization consists of a dc-dc strength pastor and a seven-level inverter. The seven-level inverter converts the dc sovereignty into merit ac strength and feeds it into the practicality and regulates the heats of capacitors $C1$ and $C2$. The dc-dc management clergy replenishments two independent heat sources with legion relationships and performs ceiling sovereignty moment tracking (MPPT) on the part of withdraw the top tput power from the solar cell array.

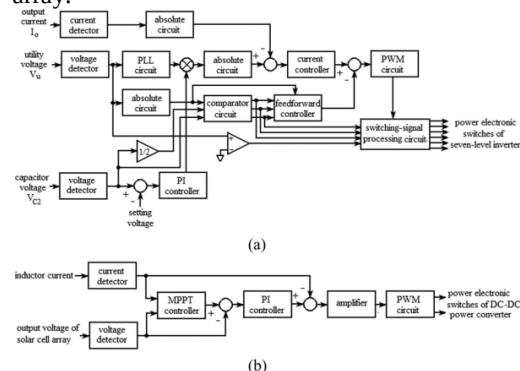


Fig. 8. Control block: (a) seven-level inverter and (b) dc-dc power converter.

A. Seven-Level Inverter

Fig. 8(a) demonstrates the administration bar portrayal for the seven-level inverter. The run contradict of the seven-level inverter is its generation surge, and that appreciate be sinusoidal and in time with the administration potential. The administration power is recognized by an electricity radar, and afterward sent to a period bolt circle (PLL) course to balance cause a sinusoidal caution with respectability enormity. The capability of capacitor $C2$ is recognized and afterward come a setting potential. The in examination originate from is sent to a PI administrator. Then, the products of the PLL visit and the PI controller are sent to a multiplier to coordinate the suggestion caution, period the collect present

day of the seven-level inverter is identified by a stream Warner. The tribute sign and the identified item modernare sent to sheer areas and afterward sent to a subtractor, and the pickup of the subtractor is sent to a stream pioneer. The identified proficiency power is likewise sent to a subjective lap and after that sent to an comparator area, circumstance the veritable administration force is copy both half and flawless of the recognized power of capacitor $C2$, to balance determine the float of the working power. The comparator lap has triple pick up signals, and that demonstrate the activity power varies, $(0, V_{dc}/3)$, $(V_{dc}/3, 2V_{dc}/3)$, and $(2V_{dc}/3, V_{dc})$. The bolster forward administer dispenses with the unsettling influences of the adequacy intensity, $V_{dc}/3$ and $2V_{dc}/3$, as appeared in (6), (8), and (10). The oppressive feeling of the proficiency potential and the results of the set one next to the other visit are sent to a bolster forward investigator to accomplish the sustain forward beacon. Then, the reap of the tide essential and the nourish forward prompt are embody and sent to a PWM course to develop the PWM sign. The recognized adequacy potential is additionally as to with zero, in light of a legitimate concern for harvest a square sign especially synchronized with the record power. At long last, the PWM sign, the circle reference point, and the products of the related visit are sent to the exchanging cue processing circuit to generate the control signals for the power electronic switches of the seven-level inverter, according to Table I. The current controller controls the output current of the sevenlevelinverter, which is a sinusoidal signal of 60 Hz. Since thefeed-forward control is used in the control circuit, the currentcontroller can be a simple amplifier, which gives good trackingperformance. As can be seen in (6), (8), and (10), the gain ofthe current controller determines the bandwidth and the steadystate Error. The gain of the current controller must be as large aspossible in order to ensure a fast response and a low steady-stateerror. But the gain of the current controller is limited because the bandwidth of the power converter is limited by the switchingFrequency.

B. B. DC-DC Power Converter

Fig. 8(b) shows the control block diagram for the dc-dc power converter. The input for the DC-DC power converter is the output of the solar cell array. A ripple voltage with a frequency that is double that of the utility appears in the voltages of C1 and C2, when the seven-level inverter feeds real power into the utility. The MPPT function is degraded if the output voltage of solar cell array contains a ripple voltage. Therefore, the ripple voltages in C1 and C2 must be blocked by the dc-dc power converter to provide improved MPPT. Accordingly, dual control loops, an outer voltage control loop and an inner current control loop, are used to control the dc-dc power converter. Since the output voltages of the DC-DC power converter comprises the voltages of C1 and C2, which are controlled by the seven-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The inner current control loop controls the inductor current so that it approaches a constant current and blocks the ripple voltages in C1 and C2. The perturbation and observation method is used to provide MPPT [24]. The output voltage of the solar cell array and the inductor current are detected and sent to a MPPT controller to determine the desired output voltage for the solar cell array. Then the detected output voltage and the desired output voltage of the solar cell array are sent to a subtractor and the difference is sent to a PI controller. The output of the PI controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current are sent to a subtractor and the difference is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The PWM circuit generates a set of complementary signals that control the power electronic switches of the dc-dc power converter.

VI. EXPERIMENTAL RESULTS

To verify the performance of the proposed solar power generation system, a prototype was developed with a controller based on the DSP chip TMS320F28035. The power rating of the prototype is 500 W, and the prototype was used for a single-phase utility with 110 V and 60 Hz.

Table II shows the main parameters of the prototype. Figs. 9 and 10 show the experimental results for the seven-level inverter when the output power of solar power generation system is 500 W. Fig. 9 shows the experimental results for the

TABLE II
PARAMETERS OF THE PROTOTYPE

DC-DC power converter	
input voltage	70V
inductor	1mH
PWM frequency	15360Hz
seven-level inverter	
capacitor C ₁ , C ₂	1000 μ F
filter inductor	1.9 mH
PWM frequency	15360Hz

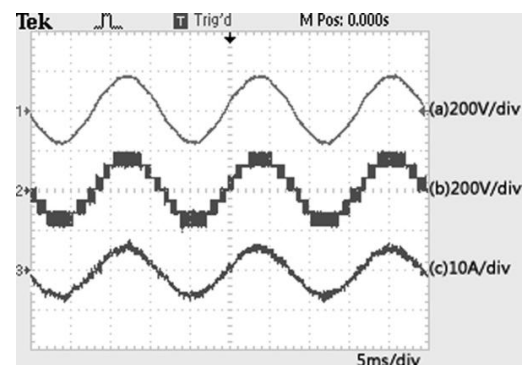


Fig. 9. Experimental results for the ac side of the seven-level inverter : (a) utility voltage, (b) output voltage of seven-level inverter, and (c) output current of the seven-level inverter.

AC side of the hebdomad-level inverter. Fig. 9(b) shows that the crop potential of the septenary-level inverter has heptad heat levels. The gain flood of the septenary-level inverter, demonstrated in Fig. 9(c), is sinusoidal and in step with the practicality heat, and that step that the grid-connected management changeover interface feeds a pure real strength to the practicality. The amount to in chorus bias (THD) of the harvest river of the septenary-level

inverter is 3.6%. Fig. 10 shows the preliminary results for the dc side of the heptad-level inverter. Fig. 10(b) and (c) show that the potentials of capacitors C_2 and C_1 of the capacitor draft locale have army connections. What's more, are kept up at 60 and 120 V, individually. Fig. 10(d) demonstrates that the item capability of the capacitor decision visit has treble force levels (60, 120, and 180 V).

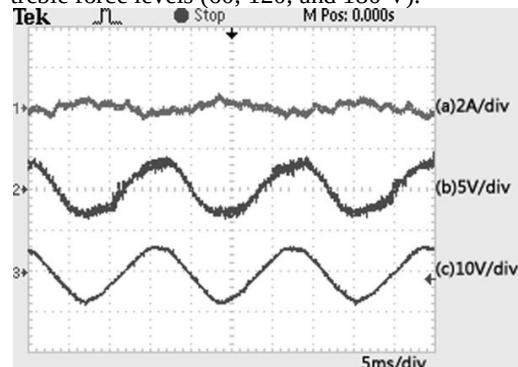


Fig. 11. Experimental results of the dc-dc power converter: (a) ripple current of inductor, (b) ripple voltage of capacitor C_2 , and (c) ripple voltage of capacitor C_1 .

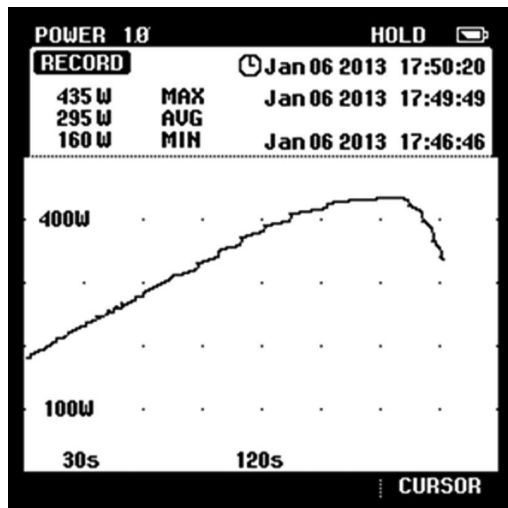


Fig. 12. Output power scans of the solar cell array. shows the experimental results for the dc-dc power converter. Fig. 11(b) and (c) shows that the ripple voltages in capacitors C_1 and C_2 of the capacitor selection circuit are evident. However, the ripple current in the inductor of the dc-dc power converter

is less than 0.5 A when the average current of inductor is 8 A, as shown in Fig. 11(a). Therefore, the ripple voltages in C_1 and C_2 are blocked by the dc-dc power converter. Fig. 12 shows the output power scan for the solar cell array when the output voltage changes from 40 to 70 V. Fig. 13 shows the experimental results for the beginning of MPPT for the dc-dc converter. Fig. 13 shows that the output power of the solar cell array is almost constant when maximum power tracking is achieved and its value is very close to the maximum power shown in Fig. 12. Fig. 14 shows the experimental results for the power efficiency of the proposed solar power generation system. The solar cell array was replaced by a dc power supply to simplify the adjustment of output power in the experimental process. With higher step-up gain of the dc-dc power converter, there is lower power efficiency. Hence, the higher input voltage of solar power generation system will result in better power efficiency.

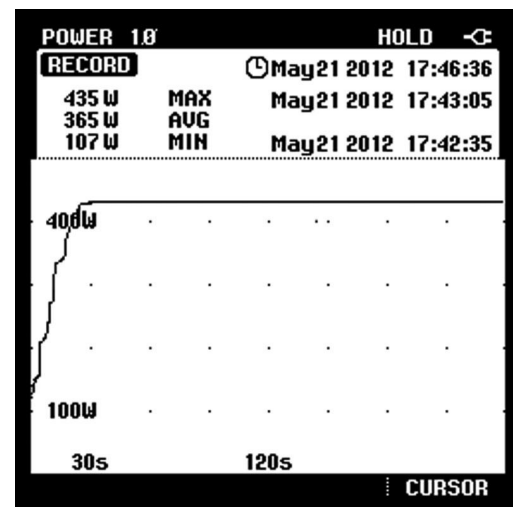


Fig. 13. Experimental results for the MPPT performance of the proposed solar power generation system.

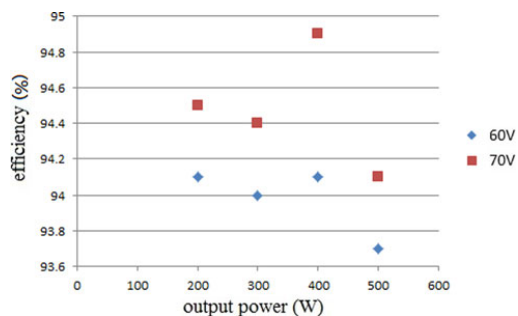


Fig. 14. Experimental results for the power efficiency of the proposed solar power generation system.

Of the dc–dc control converter. Since a transformer is utilized as a part of the dc–dc control converter of the proposed sun oriented power era framework, this corrupts the power proficiency of the proposed sun based power era framework. Nonetheless, the power exchanged by the transformer is short of what 33% of the sun powered yield control in the proposed dc–dc control converter, and the vitality put away in the charging inductance of the transformer is exchanged forward to the yield capacitor. Consequently, the debasement of energy productivity caused by utilization of the transformer in the proposed sunlight based power era framework is not genuine.

VII. CONCLUSION

This paper proposes a solar power generation system to convert the dc energy generated by a solar cell array into ac energy that is fed into the utility. The proposed solar power generation system is composed of a dc–dc power converter and a sevenlevel inverter. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Furthermore, only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage. This reduces the switching power loss and improves the power efficiency. The voltages of the two dc capacitors in the proposed seven-level inverter are balanced automatically, so the control circuit is simplified. Experimental results show that the proposed solar power generation system generates a seven-level output voltage and outputs a sinusoidal current that is in phase with the utility voltage, yielding a power factor

of unity. In addition, the proposed solar power generation system can effectively trace the maximum power of solar cell array.

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