

REDUCED DC-LINK VOLTAGE RATING

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ABSTRACT:

This circuit consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor[1-4], without compromising its performance. This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dclink

Capacitor[5-9]. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus..This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables Independent control of each leg of the shunt VSI with single dccapacitor[10-14]. The topology uses a capacitor in series with the

interfacing inductor of the shunt active filter, and the system

neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter[15-19]. The average switching frequency of the switches in the VSI also reduces, consequently the switching losses in the inverters reduce. Detailed design aspects of the series capacitor and VSI parameters have been discussed in the paper. A simulation study of the proposed topology has been carried out using PSCAD simulator, and the results are presented[20-25]. Experimental studies are carried out on three-phase UPQC prototype to verify the proposed topology.

EXISTING SYSTEM:

In existing system the three phase three WIRE UPQC has used. Mainly Voltage rating of dc-link

capacitor largely influences the compensation performance of an active filter[26-29]. So the dc-link voltage for the shunt active filter has much higher value than the peak value of the line-to-neutral voltage.

EXISTING SYSTEM METHODOLOGY:

The three phase three wires UPQC system used for compensation of power quality issues.

DISADVANTAGES OF EXISTING SYSTEM:

In this method the UPQC which requires more rating of series and shunt active filters[30-36]. Additionally to maintain the Low harmonics level by adding passive filters.

BLOCK DIAGRAM OF PROPOSED SYSTEM:

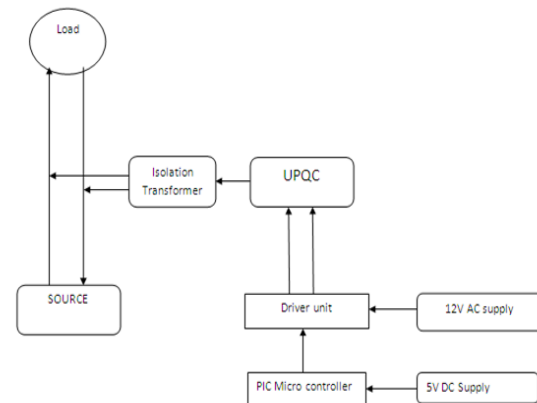


Figure.1. Proposed System Block Diagram

COMPONENTS IN THE PROPOSED SYSTEM: BASIC CONFIGURATION OF UPQC

UPQCs consist of combined series and shunt APFs for simultaneous compensation of voltage and current[37-43]. The series APF inserts a voltage, which is added at the point of common coupling (PCC) such that the load end voltage remains unaffected by any voltage disturbance, whereas, the shunt APF is most suitable to compensate for load reactive power demand and unbalance, to eliminate the harmonics from supply current, and

to regulate the common DC link voltage and to supply current[44-45]. The UPQC has two distinct parts:

Power circuit formed by series and shunt PWM Converters

UPQC controller

METHODOLOGY:

Three phase four wire UPQC system for control the Power Quality issues.

PRINCIPLE:

The UPQC is a combination of series and shunt active filters connected in cascade via a common DC link capacitor. The main purpose of a UPQC is to compensate for supply voltage power quality issues such as, sags, swells, unbalance, flicker, harmonics, and for load current power quality problems such as, harmonics, unbalance, reactive current and neutral current. A UPQC that combines the operations of a Distribution Static Compensator (DSTATCOM) and Dynamic Voltage Regulator (DVR) together.

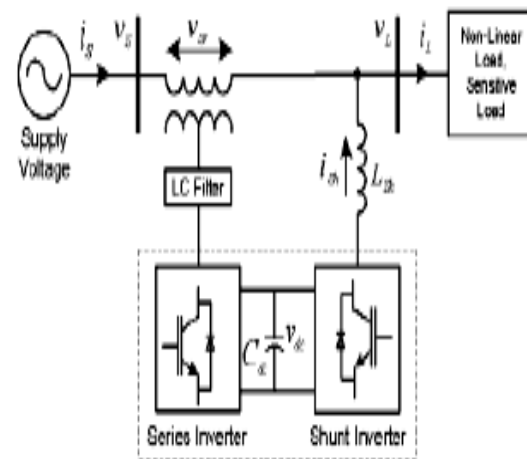


Fig.2. VSI based UPQC

CONSTRUCTION

Ultra capacitor consists of a porous electrode, electrolyte and a current collector (metal plates). There is a membrane, which separates, positive and negative plated is called separator. The following diagram shows the ultra capacitor module byarranging the individual cell.

WORKING:

- Alternating current (AC) is used for power line transmission and for high power devices like appliances and lights.

- The characteristics of AC make it ideal for transmission over long lines and for delivering large amounts of power for relatively unregulated uses, such as generating heat and light.
- Lower power appliances and devices require the closely regulated control of direct current power (DC). As a normal house is supplied with AC, it must be converted to DC for many uses.
- Two high power AC networks can be connected via a DC link, as that does not require both networks to be synchronized in frequency and phase, which is often difficult or impossible.
- DC link exists between a rectifier and an inverter, for example, in a phase converter. On one end, the utility connection is rectified into a high voltage DC. On the other end, that DC is switched to generate a new AC power waveform.
- It's a link because it connects the input and output stages. The term "DC link" is also used to describe the decoupling capacitor in the DC link. I assume that this is what you're asking about.
- The switching network on the output side generates very large transients at the switching frequency.
- The DC link capacitor helps to keep these transients from radiating back to the input. This can also help prevent the switching network from oscillating or triggering inadvertently at an inappropriate moment and causing a short.
- Additionally, if the input is not multiple-phase, the capacitor helps provide a

source of energy when the input waveform is near zero.

PERFORMANCE OF DRIVER

UNIT

- The input to a TTL circuit is always through the emitter(s) of the input transistor, which exhibits a low input resistance.
- The base of the input transistor, on the other hand, is connected to the Vcc line, which causes the input transistor to pass a current of about 1.6 mA when the input voltage to the emitter(s) is logic '0', i.e., near ground.
- Letting a TTL input 'float' (left unconnected) will usually make it go to logic '1', but such a state is vulnerable to stray signals, which is why it is good practice to connect TTL inputs to Vcc using 1 kohm pull-up resistors.

- The most basic TTL circuit has a single output transistor configured as an inverter with its emitter grounded and its collector tied to Vcc with a pull-up resistor, and with the output taken from its collector.

POWER MOSFET:

The MOSFET, or Metal-Oxide-Semiconductor Field-Effect Transistor is far the most common field effect transistor in both digital and analog circuits. The MOSFET is composed of a channel of n-type or p-type semiconductor material, and is accordingly called an NMOSFET or a PMOSFET. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good gate oxides and thus are not suitable for MOSFETs.

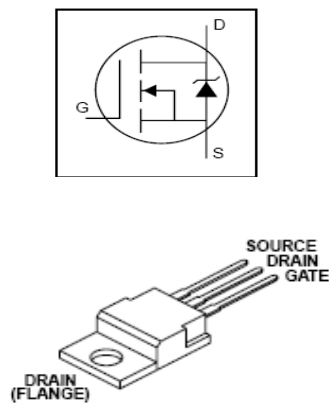


Fig 3. Power MOSFET

FEATURES OF POWER MOSFET:

- Power MOSFET has lower switching losses but its on-resistance and conduction losses are more.

BIDIRECTIONAL DC-DC CONVERTER:

The bidirectional dc to dc converter along with energy storage has become a promising option for many power related system including power related systems and hybrid electric vehicles. It is not only reducing the cost and improving the efficiency. MOSFET is the switches used in the converter. In this

T_1, T_2, T_3, T_4 are the switches used in the inverter bridge side and T_5, T_6, T_7, T_8 are the switches used in the rectifier side. Where L is the leakage inductance used for the soft switching and the values for the leakage inductance is $27 \mu\text{H}$, the capacitors C_{dc1} , C_{dc2} used for the filtering purpose

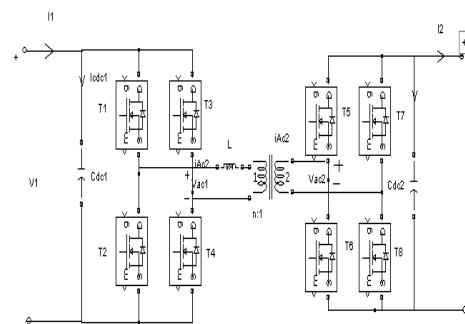


Fig 4. Bidirectional dc-dc converter circuit diagram

- In ,Dual active-bridge bi-directional dc-dc converter, the one full bridge serves as High Frequency (HF) inverter and the other full bridge serves as rectifier.

OPERATING PRINCIPLE

The operating principle of the proposed system can be explained by the following modes of operation

MODES OF OPERATION

MODE1:

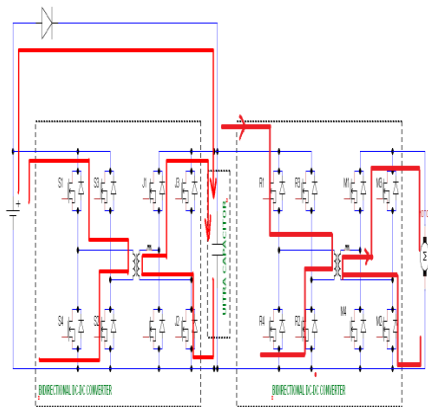


Fig 5. Energy flow of the Acceleration mode phase I

In Mode1 energy from the battery is directly supplied to Dual active bridge converter2(DAB2) and from DAB2 the energy is supplied to the motor and it starts running, meanwhile charging takes place in Ultra capacitor from battery through DAB1.

MODE 2

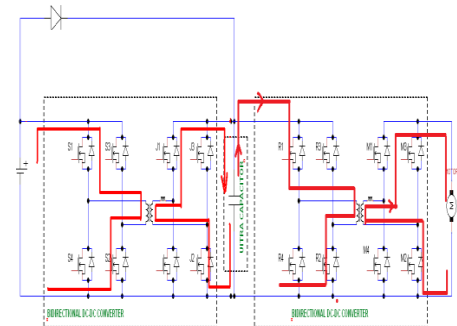


Fig 6. Energy flow of the Acceleration mode phase II

In Mode2 the motor draws energy from Ultra capacitor through Dual active bridge2. In this mode vehicle speed is increased.

MODE 3

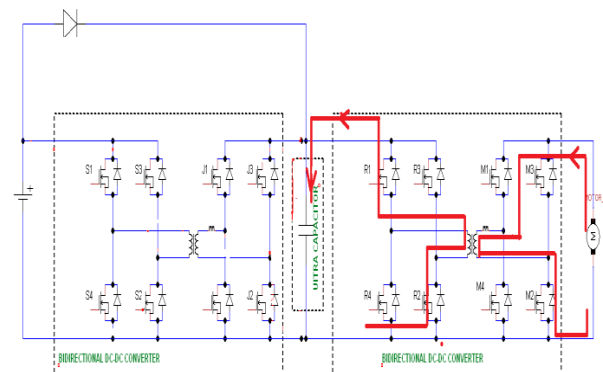


Fig 7. Energy flow of Regenerative braking phase I

In Mode 3 the excess energy from the motor is stored in ultra capacitor through Dual active bridge 2.

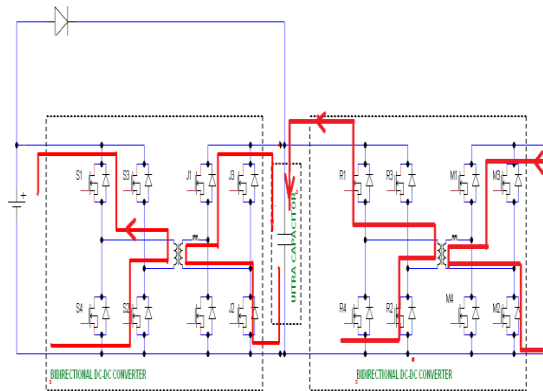
MODE 4

Fig 8. Energy flow of Regenerative braking phase II

In this mode when ultra capacitor is fully charged the energy from the motor is stored in battery through Dual active bridge1.

V_{in} is the input voltage

$$V_0 = 6V$$

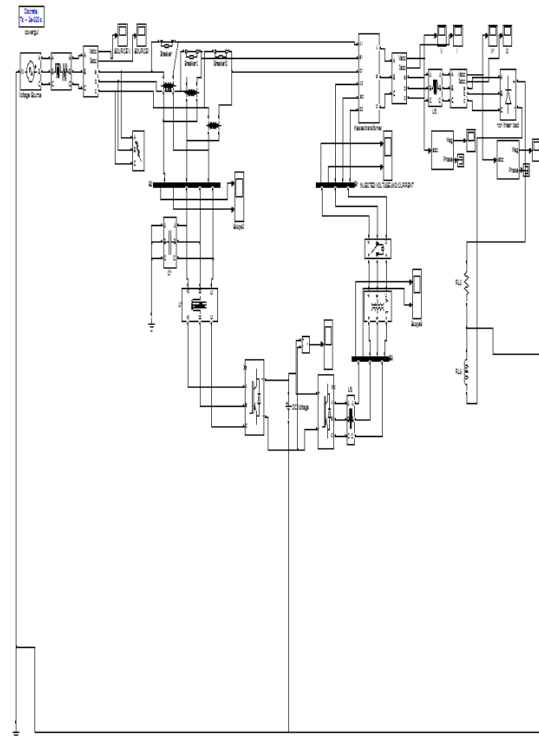
SIMULINK RESULTS:**SIMULINK MODEL**

Fig 9. Simulink Diagram

OPTOCOUPLEDERS

The most important parameter for most Optocouplers is their transfer efficiency, usually measured in terms of their current transfer ratio or CTR. This is simply the ratio between a current change in the output transistor and the current change in the input LED which produced it. Typical values for CTR range from 10% to 50% for devices with an output phototransistor and

up to 2000% or so for those with a Darlington transistor pair in the output. Note, however that in most devices CTR tends to vary with absolute current level. Typically it peaks at a LED current level of about 10mA, and falls away at both higher and lower current levels. Other optocoupler parameters include the output transistor's maximum collector-emitter voltage rating $V_{CE}(\max)$, which limits the supply voltage in the output circuit; the input LED maximum current rating $I_F(\max)$, which is used to calculate the minimum value for its series resistor; and the Optocouplers bandwidth, which determines the highest signal frequency that can be transferred through it ó determined mainly by internal device construction and the performance of the output Phototransistor.

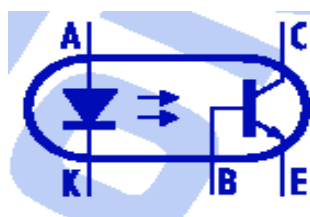


Fig 10.Optocoupler

SIMULATION RESULT:

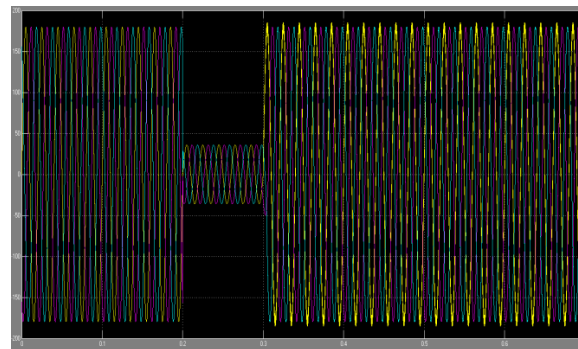


Fig 11.Output voltage with voltage sag

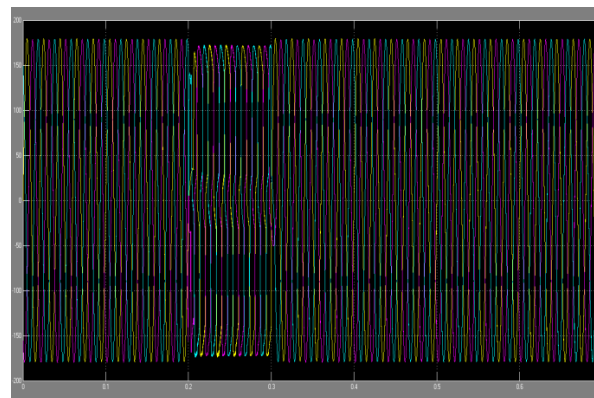


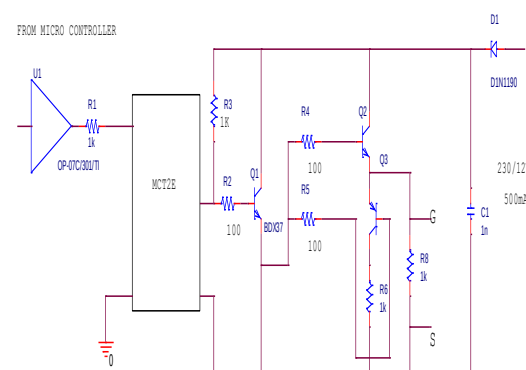
Fig 12.Output voltage after eliminating voltage sag

CONCLUSION

A modified UPQC topology for three-phase four-wire system has been proposed in this paper, which

topology (conventional). The proposed modified topology gives the advantages of both the conventional neutral-clamped topology and the four-leg topology. Detailed comparative studies are made for the conventional and modified topologies. From the study, it is found that the modified topology has less average switching frequency, less THDs in the source currents, and load voltages with reduced dc-link voltage as compared to the conventional UPQC topology.

DRIVER CIRCUIT



- 2% internal oscillator
- Programmable PLL and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer

- Low-power management modes
- Fast wake-up and start-up

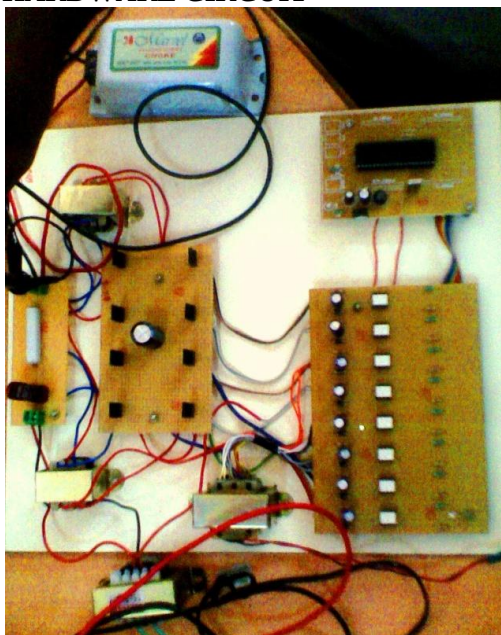
Core Performance

- Up to 40 MIPS 16-bit dsPIC33F CPU
- Two 40 bit wide accumulators
- Single-cycle (MAC/MPY) with dual data fetch
- Single-cycle MUL plus hardware divide

Motor Control PWM

- Up to four PWM generators with eight outputs
- Dead Time for rising and falling edges
- 25 ns PWM resolution
- PWM support for Motor Control: BLDC, PMSM, ACIM, and SRM
- Programmable Fault inputs
- Flexible trigger for ADC conversions and configurations.

HARDWARE CIRCUIT



CONCLUSION

A modified UPQC topology for three-phase four-wire system has been proposed in this paper, which has the capability to compensate the load at a lower dc-link voltage under nonstiff source. Design of the filter parameters for the series and shunt active filters is explained in detail. The proposed method is validated through simulation and experimental studies in a three-phase distribution system with neutral-clamped UPQC

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REFERENCES

1. Nimal, R.J.G.R., Hussain, J.H., Effect of deep cryogenic treatment on EN24 steel, International Journal of Pure and Applied Mathematics, V-116, I-17 Special Issue, PP-113-116, 2017
2. Parameswari, D., Khanaa, V., Deploying lampport clocks and linked lists, International Journal of Pharmacy and Technology, V-8, I-3, PP-17039-17044, 2016
3. Parameswari, D., Khanaa, V., Case for massive multiplayer online role-playing games, International Journal of Pharmacy and Technology, V-8, I-3, PP-17404-17409, 2016
4. Parameswari, D., Khanaa, V., Deconstructing model checking with hueddot, International Journal of Pharmacy and Technology, V-8, I-3, PP-17370-17375, 2016
5. Parameswari, D., Khanaa, V., The effect of self-learning epistemologies on theory, International Journal of Pharmacy and Technology, V-8, I-3, PP-17314-17320, 2016
6. Pavithra, J., Peter, M., GowthamAashirwad, K., A study on business process in IT and systems through extranet, International Journal of Pure and Applied Mathematics, V-116, I-19 Special Issue, PP-571-576, 2017
7. Pavithra, J., Ramamoorthy, R., Satyapira Das, S., A report on evaluating the effectiveness of working capital management in googolsoft technologies, Chennai, International Journal of Pure and Applied Mathematics, V-116, I-14 Special Issue, PP-129-132, 2017
8. Pavithra, J., Thooyamani, K.P., A cram on consumer behaviour on Mahindra two wheelers in Chennai, International Journal of Pure and Applied Mathematics, V-116, I-18 Special Issue, PP-55-57, 2017
9. Pavithra, J., Thooyamani, K.P., Dkhar, K., A study on the air freight customer satisfaction, International Journal of Pure and Applied Mathematics, V-116, I-14 Special Issue, PP-179-184, 2017
10. Pavithra, J., Thooyamani, K.P., Dkhar, K., A study on the working capital management of TVS credit services limited, International Journal of Pure and Applied Mathematics, V-116, I-14 Special Issue, PP-185-187, 2017
11. Pavithra, J., Thooyamani, K.P., Dkhar, K., A study on the analysis of financial performance with reference to Jeppiaar Cements Pvt Ltd, International Journal of Pure and Applied Mathematics, V-116, I-14 Special Issue, PP-189-194, 2017
12. Peter, M., Dayakar, P., Gupta, C., A study on employee motivation at Banalari World Cars Pvt Ltd Shillong, International Journal of Pure and Applied Mathematics, V-116, I-18 Special Issue, PP-291-294, 2017
13. Peter, M., Kausalya, R., A study on capital budgeting with reference to signware technologies, International Journal of Pure and Applied Mathematics, V-116, I-18 Special Issue, PP-71-74, 2017
14. Peter, M., Kausalya, R., Akash, R., A study on career development with reference to premheerasurgicals, International Journal of Pure and Applied Mathematics, V-116, I-14 Special Issue, PP-415-420, 2017
15. Peter, M., Kausalya, R., Mohanta, S., A study on awareness about the cost reduction and elimination of waste among employees in life line multispeciality hospital, International Journal of Pure and Applied

- Mathematics, V-116, I-14 Special Issue, PP-287-293, 2017
16. Peter, M., Srinivasan, V., Vignesh, A., A study on working capital management at deccan Finance Pvt Limited Chennai, International Journal of Pure and Applied Mathematics, V-116, I-14 Special Issue, PP-255-260, 2017
 17. Peter, M., Thooyamani, K.P., Srinivasan, V., A study on performance of the commodity market based on technical analysis, International Journal of Pure and Applied Mathematics, V-116, I-18 Special Issue, PP-99-103, 2017
 18. Philomina, S., Karthik, B., Wi-Fi energy meter implementation using embedded linux in ARM 9, Middle - East Journal of Scientific Research, V-20, I-12, PP-2434-2438, 2014
 19. Philomina, S., Subbulakshmi, K., Efficient wireless message transfer system, International Journal of Pure and Applied Mathematics, V-116, I-20 Special Issue, PP-289-293, 2017
 20. Philomina, S., Subbulakshmi, K., Ignition system for vehicles on the basis of GSM, International Journal of Pure and Applied Mathematics, V-116, I-20 Special Issue, PP-283-286, 2017
 21. Philomina, S., Subbulakshmi, K., Avoidance of fire accident by wireless sensor network, International Journal of Pure and Applied Mathematics, V-116, I-20 Special Issue, PP-295-299, 2017
 22. Pothumani, S., Anuradha, C., Monitoring android mobiles in an industry, International Journal of Pure and Applied Mathematics, V-116, I-20 Special Issue, PP-537-540, 2017
 23. Pothumani, S., Anuradha, C., Decoy method on various environments - A survey, International Journal of Pure and Applied Mathematics, V-116, I-10 Special Issue, PP-197-199, 2017
 24. Pothumani, S., Anuradha, C., Priya, N., Study on apple iCloud, International Journal of Pure and Applied Mathematics, V-116, I-8 Special Issue, PP-389-391, 2017
 25. Pothumani, S., Hameed Hussain, J., A novel economic framework for cloud and grid computing, International Journal of Pure and Applied Mathematics, V-116, I-13 Special Issue, PP-5-8, 2017
 26. Pothumani, S., Hameed Hussain, J., A novel method to manage network requirements, International Journal of Pure and Applied Mathematics, V-116, I-13 Special Issue, PP-9-15, 2017
 27. Pradeep, R., Vikram, C.J., Naveenchandra, P., Experimental evaluation and finite element analysis of composite leaf spring for automotive vehicle, Middle - East Journal of Scientific Research, V-12, I-12, PP-1750-1753, 2012
 28. Prakash, S., Jayalakshmi, V., Power quality improvement using matrix converter, International Journal of Pure and Applied Mathematics, V-116, I-19 Special Issue, PP-95-98, 2017
 29. Prakash, S., Jayalakshmi, V., Power quality analysis & power system study in high voltage systems, International Journal of Pure and Applied Mathematics, V-116, I-19 Special Issue, PP-47-52, 2017
 30. Prakash, S., Sherine, S., Control of BLDC motor powered electric vehicle using indirect vector control and sliding mode observer, International Journal of Pure and Applied Mathematics, V-116, I-19 Special Issue, PP-295-299, 2017
 31. Prakesh, S., Sherine, S., Forecasting methodologies of solar resource and PV power for smart grid energy

- management, International Journal of Pure and Applied Mathematics, V-116, I-18 Special Issue, PP-313-317, 2017
32. Prasanna, D., Arulselvi, S., Decoupling smalltalk from rpcs in access points, International Journal of Pure and Applied Mathematics, V-116, I-16 Special Issue, PP-1-4, 2017
 33. Prasanna, D., Arulselvi, S., Exploring gigabit switches and journaling file systems, International Journal of Pure and Applied Mathematics, V-116, I-16 Special Issue, PP-13-17, 2017
 34. Prasanna, D., Arulselvi, S., Collaborative configurations for wireless sensor networks systems, International Journal of Pure and Applied Mathematics, V-116, I-15 Special Issue, PP-577-581, 2017
 35. Priya, N., Anuradha, C., Kavitha, R., Li-Fi science transmission of knowledge by way of light, International Journal of Pure and Applied Mathematics, V-116, I-9 Special Issue, PP-285-290, 2017
 36. Priya, N., Pothumani, S., Kavitha, R., Merging of e-commerce and e-market-a novel approach, International Journal of Pure and Applied Mathematics, V-116, I-9 Special Issue, PP-313-316, 2017
 37. Raj, R.M., Karthik, B., Effective demining based on statistical modeling for detecting thermal infrared, International Journal of Pure and Applied Mathematics, V-116, I-20 Special Issue, PP-273-276, 2017
 38. Raj, R.M., Karthik, B., Energy sag mitigation for chopper, International Journal of Pure and Applied Mathematics, V-116, I-20 Special Issue, PP-267-270, 2017
 39. Raj, R.M., Karthik, B., Efficient survey in CDMA system on the basis of error revealing, International Journal of Pure and Applied Mathematics, V-116, I-20 Special Issue, PP-279-281, 2017
 40. Rajasulochana, P., Krishnamoorthy, P., Ramesh Babu, P., Datta, R., Innovative business modeling towards sustainable E-Health applications, International Journal of Pharmacy and Technology, V-4, I-4, PP-4898-4904, 2012
 41. Rama, A., Nalini, C., Shanthi, E., An iris based authentication system by eye localization, International Journal of Pharmacy and Technology, V-8, I-4, PP-23973-23980, 2016
 42. Rama, A., Nalini, C., Shanthi, E., Effective collaborative target tracking in wireless sensor networks, International Journal of Pharmacy and Technology, V-8, I-4, PP-23981-23986, 2016
 43. Ramamoorthy, R., Kanagasabai, V., Irshad Khan, S., Budget and budgetary control, International Journal of Pure and Applied Mathematics, V-116, I-20 Special Issue, PP-189-191, 2017
 44. Ramamoorthy, R., Kanagasabai, V., Jivandan, S., A study on training and development process at Vantec Logistics India Pvt Ltd, International Journal of Pure and Applied Mathematics, V-116, I-14 Special Issue, PP-201-207, 2017.
 45. Pradeep, R., Vikram, C.J., Naveenchandran, P., Experimental evaluation and finite element analysis of composite leaf spring for automotive vehicle, Middle - East Journal of Scientific Research, V-17, I-12, PP-1760-1763, 2013

