

A RESONANT DC/DC CONVERTER USING AN AUXILIARY CIRCUIT TOPOLOGY

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Abstract— A pulse width adjusted full dc/dc converter utilizing an auxiliary circuit will be proposed in this paper. The auxiliary circuit comprises of a system of two capacitors and an inductor. Utilizing Metal Oxide Semiconductor Field Effect Transistors (MOSFET) as synchronous rectifiers can encourage diminish power misfortunes and enhance the efficiency. The circuit outline for filter PWM full DC/DC converter is drawn and the circuit is reenacted by utilizing MATLAB.

Index Terms—Auxiliary circuit, capacitor, dc/dc converter, inductor, MOSFET, pulse-width-modulated.

I. INTRODUCTION

Coordinated force supplies are required for most clear and advanced electronic structures. Power supplies which are broadly utilized as a bit of mechanical applications are required to oversee yield, low music[1-4], low swells, diminishing in size and weight and high profitability.. The single stage converter does not meet a large portion of these particulars and multistage changes are regularly required. Subordinate upon the kind of yield voltage power supplies can be asked for into two sorts[5-9].

1. DC power supplies

2. Air conditioning power supplies

For the most part direct power supplies have

been used. However pushes in semi conductor development have lead to trading power supplies which are humbler in size and in a general sense more gainful emerged from straight power supplies[10-15]. Due to straight impact supplies they require a transistor joined in course of action which works in component domain results epic measure of force incident and the over all amplex is low.

Different systems for high rehash change have been proposed to diminish the part push of Voltage and Current and the exchanging incidents in the standard Pulse width modulated(PWM) converter A novel Zero-voltage and Zero current exchanging (ZVZCS) three level DC-DC converter beat the shortcomings appeared by the typical Zero voltage exchanging (ZVS) three level converter[16-19]. For example,

1. High circulating energy.

2. Sever parasitic ringing on the rectifier diode.

3. Limited ZVS load range for the inner switches

This converter uses a stage shift control with flying capacitor in the essential side to accomplish ZVS for the external switches. The converter uses a helper circuit to reset the essential current amid the free wheeling stage to accomplish zero current exchanging (ZCS) for the internal switches[20-26].

NEED FOR DC-DC CONVERTER

Variable rate dc drives are as a result dynamically used as a piece of every business enterpris. These drives and shapes take power from dc voltage sources. A dc-dc converter changes over direct from dc-dc and is fundamentally known as dc converter. A dc converter can be considered as dc proportionate to an aeration and cooling system transformer with an always variable turns extent[27-31]. Like a transformer it can be used to wander down or wander up a dc voltage source.

DC converters are for the most part used for balance motor control as a piece of electric autos, trolley automobiles, marine derricks and mine haulers. They give smooth expanding speed control, high profitability, lessened size and weight and fast component response[32-37]. Dc converters can be used as a piece of regenerative breaking of dc motors to return imperativeness afresh into the supply and this segment results in essentialness venture reserves for transportation structures with relentless stops.

BLOCK DIAGRAM EXPLANATION

The AC source is given to rectifier circuit which converts ac to dc .the filter circuit eliminate the ripples from the incoming dc signal. This dc signal is given as input to the PWM dc to dc converter .the semiconducting devices in this converter is controlled by the PWM pulses. This PWM pulses are generated by the microcontroller[38-41]. Then the Dc to Dc converter controls the dc load.

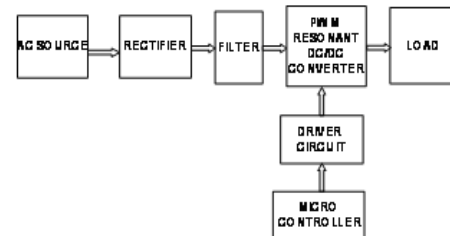


Fig. 1 BLOCK DIAGRAM

TYPES OF SWITCHING

- 1) Hard switching
- 2) Soft switching
 - i) Zero Current Switching
 - ii) Zero Voltage Switching

In hard switching, the devices are turned on and off without making the current through or voltage across them as zero. Hence switching losses will be more and size of the component will be large. Also conversion efficiency is low. In soft switching, the devices are turned on and off while the current and/ or voltage across them as zero. Hence switching losses will be less and size of the component will be small. Also conversion efficiency is improved.

ZERO VOLTAGE SWITCHING

In ZCS the semiconductor switches are on and off by making current through the switch is zero. Be that as it may, in ZVS the exchanging gadgets are made to kill on and turn the whole load current at high di/dt. The gadgets taking care of high di/dt likewise encounter high voltage stresses crosswise over them[42-45]. Because of these two impacts there are expanded force misfortunes in the exchanging gadgets. In the event that size and weight of the converter parts is to be decreased,

exchanging frequencies are expanded. At these high frequencies exchanging misfortunes and high voltage burdens are further disturbed. Another significant inconvenience of high di/dt and high dv/dt brought about by fast on and off of the exchanging gadgets is the electro attractive obstruction.

The impediments specified above can be minimized if every switch in a converter is turned on and off when the voltage crosswise over it is zero at the moment of exchanging. This kind of converter is called thunderous converters.

Fundamental REQUIREMENTS OF ZVS

The turn off time ought to be sufficiently expansive to totally charge or release the capacitors over the gadgets. There ought to be time delay between the turn off a gadget and turn off the integral gadget on the same leg. The time postponement ought to be sufficient to permit the complete charge or release the capacitor over the gadgets.

Working PRINCIPLE OF THE CONVERTER

The accompanying presumptions are made to streamline the investigation of the converter. The circuit operation is in relentless state. The yield channel inductor is sufficiently huge to be considered as a present source. Every one of the gadgets perfect and the transformer polarizing current is disregarded. Capacitances paralleled with switches incorporate parasitic capacitances and outer capacitances, and every one of the capacitances are equivalent qualities.

II. CIRCUIT DIAGRAM

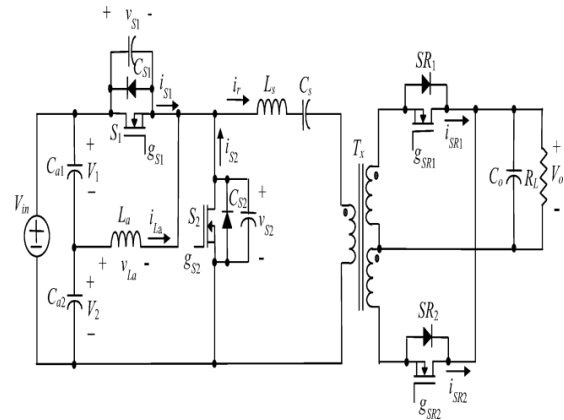


Fig. 2. Modified APWM series resonant dc/dc converter topology.

The asymmetrical pulse-width-modulated (APWM) resonant Dc/Dc converter topology has been presented and it offers near-zero switching losses while operating at constant and very high frequencies. Its segment tally is low, making operation, at low to medium force levels attainable. The information voltage range over which ZVS is accomplished is restricted, and the productivity of the converter declines as the data voltage is expanded. Additionally, the full inductor causes higher misfortunes as the working recurrence is expanded. This paper shows an adjusted APWM full dc/dc topology (Fig. 2) that can defeat the downsides portrayed previously. Fig. 2 demonstrates an APWM resounding dc/dc converter topology utilizing the extra system. This circuit can be broken into practical obstructs: the assistant circuit (C_{1a}, C_{s2}, L_a), a chopper (S_1, S_2), an arrangement resounding tank (L_a, C_a), a force transformer (T_x), Synchronous rectifier (SR_1, SR_2) and the yield channel. The assistant circuit has the accompanying capacities:

- i) inductor provides compensating current to achieve ZVS at higher input voltage.

ii) Capacitors C1a and C2a split the dc input voltage.

OPERATING PRINCIPLE

This circuit contains two switches, S1 and S2 which are controlled by two reimbursing gating signals, $gs1$ and $gs2$, independently. The gating indication of S1 has a commitment cycle D of and that of S2 is $1-D$. Right when is on, the power from the source is traded to the stack and the yield of the chopper sees a positive voltage of V_{in} from the source. Exactly when S2 turns on, the source is disconnected from whatever is left of the power circuit and the yield of the chopper sees the voltage across over S2 which is zero volts.

The imperativeness from the full fragments now freewheels through and Supplies vitality to the pile. By moving D we can control the yield voltage. This requires a feedback framework, which fabricates D if the yield Voltage ends up being too low and the a different way.

The operation of this circuit can be found in four interims. Fig. 3 demonstrates the key waveforms amid each of these interims. For every interim, the operation of the converter is portrayed as takes after,

Interim I

Preceding this interim S2 was on, and toward the start of this interim, S2 is exchanged off. The negative current coursing through the thunderous branch and the positive current through the assistant inductor drive the charging of C2 and the releasing of C1. Once C1 has completely released and C2 has completely charged, the present powers the conduction of diode D1. The voltage crosswise over S1 is currently set at 0 volts, and the voltage across S2

measures up to V_{in} . In the mean time, the voltage crosswise over La changes from

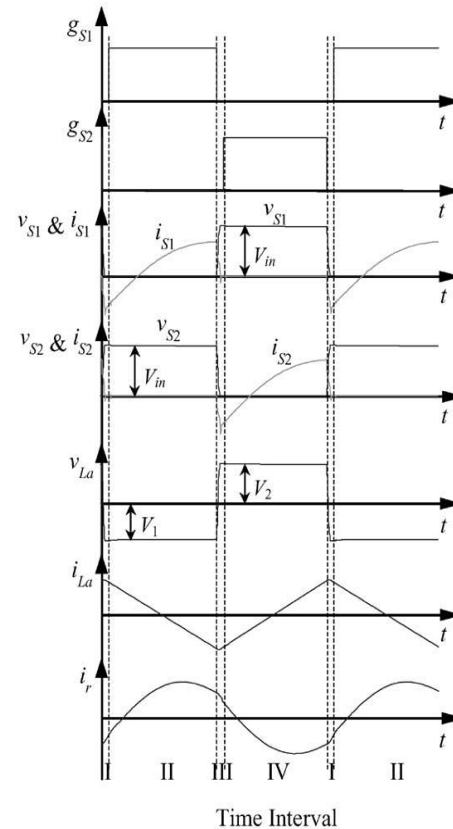


Fig. 3. Key operating waveforms of the circuit diagram in Fig. 2.

($+V_2$) to ($-V_1$). V_1 and V_2 are the voltages across C_{a1} and C_{a2} , respectively. The current through during this interval reaches its peak value and starts to decrease.

Interval I

Toward the start of this interim, gating signal $gs1$ is connected to the door of S1 to switch it on. The current already coursing through D1 now moves through S1. The switch along these lines turns on under zero voltage, and the yield voltage of the chopper equivalents V_{in} . Power streams from the info dc source to the full circuit and to the yield load. The voltage crosswise over La

amid this interim stays consistent at $(-V_1)$, and the current through L_a continues diminishing directly.

Interim III

Toward the start of this interim, switch S_1 is killed. The positive current coursing through the deafening branch and the negative current through the associate inductor constrain the discharging of C_2 and the charging of C_1 . Once C_2 has totally discharged and C_1 has totally charged,

The present powers the conduction of diode D_2 . The voltage across over S_2 is as of now set at 0 volts, and the voltage transversely over S_1 counterparts V_{in} . In the meantime, the voltage transversely over L_a changes from $(-V_1)$ to $(+V_2)$, and the current through L_a accomplishes its negative peak regard and starts to increase.

Interim IV

Toward the start of this interim, gating signal gs_2 is connected to the entryway of S_2 to switch it on. The current already moving through D_2 now moves through S_2 . The switch along these lines turns on under zero voltage, and the yield voltage of the chopper is braced to zero. The vitality put away in the full parts now courses through S_2 to supply energy to the yield load. The voltage crosswise over L_a amid this interim stays consistent at $(+V_2)$, and the current through L_a continues expanding directly.

2. Consistent STATE ANALYSIS OF THE CONVERTER

This area will show the enduring state investigation of the circuit in Fig. 2. In doing the examination, the accompanying

presumptions are made.

- 1) The semiconductor switches and diodes are perfect.
- 2) The impact of capacitors over the switches is unimportant.
- 3) An air conditioner proportional resistance at the essential of transformer speaks to the yield correction stage.
- 4) The deferral time between the two switches is ignored.
- 5) The diode rectifier causes zero misfortunes.

The base info voltage, $V_{in,min}$ (volts), the comparable AC resistance R_{ac} and the resounding recurrence of the arrangement thunderous parts are picked as the base qualities. The accompanying mathematical statements have been created from the first circuit, however are still legitimate for this topology.

Interval III

At the beginning of this interval, switch S_1 is turned off. The positive current coursing through the thunderous branch and the negative current through the assistant inductor compel the releasing of C_2 and the charging of C_1 . Once C_2 has completely released and C_1 has completely charged,

The present powers the conduction of diode D_2 . The voltage crosswise over S_2 is currently set at 0 volts, and the voltage crosswise over S_1 equivalents V_{in} . In the interim, the voltage crosswise over L_a changes from $(-V_1)$ to $(+V_2)$, and the current through L_a achieves its negative

crest esteem and begins to increment.

Interval IV

Toward the start of this interim, gating signal gs_2 is connected to the entryway of S2 to switch it on. The current beforehand coursing through D2 now moves through S2. The switch in this manner turns on under zero voltage, and the yield voltage of the chopper is braced to zero. The vitality put away in the full segments now moves through S2 to supply energy to the yield load. The voltage crosswise over La amid this interim stays steady at $(+V_2)$, and the current through La continues expanding straightly.

2. STEADY-STATE ANALYSIS OF THE CONVERTER

This section will present the steady-state analysis of the circuit in Fig. 2. In doing the analysis, the following assumptions are made.

- 1) The semiconductor switches and diodes are ideal.
- 2) The effect of capacitors across the switches is negligible.
- 3) An ac equivalent resistance at the primary of transformer represents the output rectification stage.
- 4) The delay time between the two switches is neglected.
- 5) The diode rectifier incurs zero losses.

The minimum input voltage, $V_{in,min}$ (volts), the equivalent AC resistance R_{ac} and the resonant frequency of the series resonant components are chosen as the base values. The following equations have been developed from the original circuit, but are still valid for this topology

$$Q_0 = \omega_r L_s / R_{ac} \quad (1)$$

$$\omega = \omega_0 / \omega_r$$

$$(2)$$

$$R_{ac} = (8/\pi^2) * N^2 * R_L \quad (3)$$

$$f_r = 1/(2\pi * (L_s C_s)^{1/2})$$

$$(4) \quad (4)$$

Where ω_0 is the working recurrence, R_L is the load resistance, N is the turns proportion of the transformer, and L_s and C_s are the series inductance and capacitance, individually. With a specific end goal to streamline the examination, the circuit can be separated into its utilitarian pieces. Comparison (3) demonstrates how the yield burden is seen as an air conditioner equal resistance by the resonating tank. An equal model of the yield stage is appeared in Fig. 4. The following stage is the full tank system. The voltage at the information of the full tank is equivalent to the voltage, V_{s2} , over the switch S2. This can be spoken to regarding Fourier arrangement in one exchanging cycle T_s as

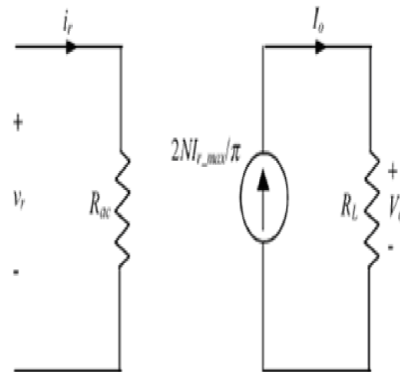


Fig. 4. Equivalent Model of the ideal output Stage.

$$V_{s2}(t) = V_{in} D + \sum \left[\left(\sqrt{2} * V_{in} / n \pi \right) * \sqrt{1 - \cos 2n \pi D} * \sin(n \omega_0 t + \Theta_n) \right] \quad (5)$$

Where

$$\Theta_n = \tan^{-1} [\sin 2n \pi D / (1 - \cos 2n \pi D)] \quad (6)$$

The per unit resonant current is derived from

the ac component

Of V_{S2} , V_{S2_ac}

$$i_r(t) = \sum (\sqrt{2} V_{in}/(n\Pi |Z_{in}| V_{in, min}) * \sqrt{1 - \cos 2n\Pi D} * \sin(n\omega t + \Theta_n - \phi_n)) \quad (7)$$

Where

$$|Z_{in}| = \sqrt{1 + Q_0^2 (n\omega - 1/n\omega)^2} \quad (8)$$

$$\phi_n = \tan^{-1}[Q_0(n\omega - 1/n\omega)] \quad (9)$$

From (7), the peak value of the fundamental resonant current, I_{r_max} can be given as

$$I_{r_max} = \frac{\sqrt{2} V_{in} * \sqrt{1 - \cos 2\Pi D}}{(\Pi * V_{in} * \sqrt{1 + Q_0^2 (\omega - \frac{1}{\omega})^2})} \quad (10)$$

The equivalent model of the fundamental of the resonant tank network is shown in Fig. 5.

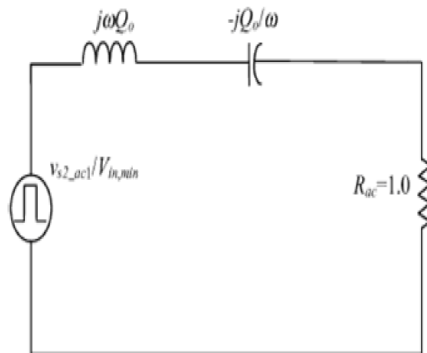


Fig .5. Fundamental Model of the DC Resonant Tank.

The next stage to be considered is the switch and the

compensating network. The switch currents are functions of both the resonant and auxiliary currents. The auxiliary inductor generates the auxiliary current. To solve for this current, the waveforms of the voltage across and current through the auxiliary inductor are redrawn in Fig. 5. Assume for simplicity that the dead time between gating signals $gs1$ and $gs2$ is zero in the following derivation.

Firstly, the voltages across the auxiliary capacitors C_{a1} and C_{a2} , V_1 and V_2 , respectively, have to be derived. Since C_{a1} and C_{a2} split the dc input voltage ($V_1 + V_2 = V_{in}$), in the steady state, V_1 and V_2 can be obtained as

$$V_1 = (1-D) V_{in} \quad (11)$$

$$V_2 = D V_{in} \quad (12)$$

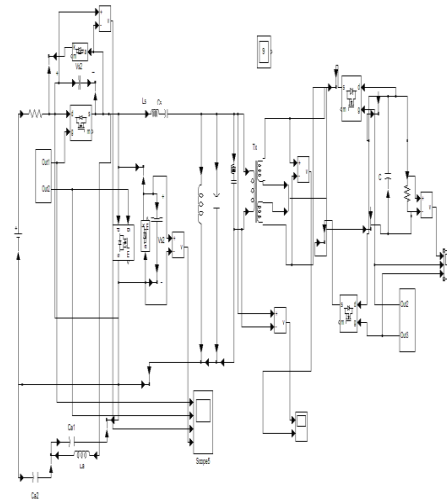
Now that each stage has been analyzed, the whole converter Can be seen in its entirety. The voltage conversion ratio, M , is the ratio between the output and the input voltages. It is given by,

$$M = \frac{V_0}{V_{in}} = \frac{2\sqrt{2}N * R_0 * \sqrt{1 - \cos(2\Pi D)}}{\Pi^2 \sqrt{1 + Q_0^2 (\omega - \frac{1}{\omega})^2}}$$

III. SIMULATION

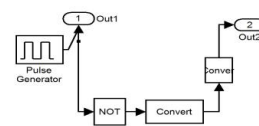
Reenactment is an activity process. It is used to think about the associations between parameters which interface in a structure. From time to time, it may point out bungles in a design which can realize the blueprint to be unworkable. In other case it gifts change of a diagram for most noteworthy execution or money related of operation or advancement. In still diverse samples, the SYSTEMS potentially so multifaceted that the amusement is the primary way in which the variables impacting the arrangement and

their correspondence with each other can be controlled and considered. This area oversees reenactment of astray PWM full converter using MATLAB programming. It has been viewed that the entertainment results are found to agree with orderly results to a measurable degree.

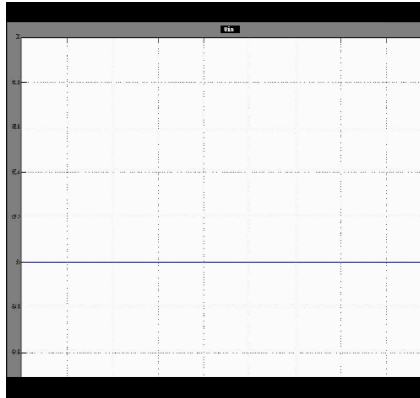


PULSEGENERATION/SUB SYSTEM

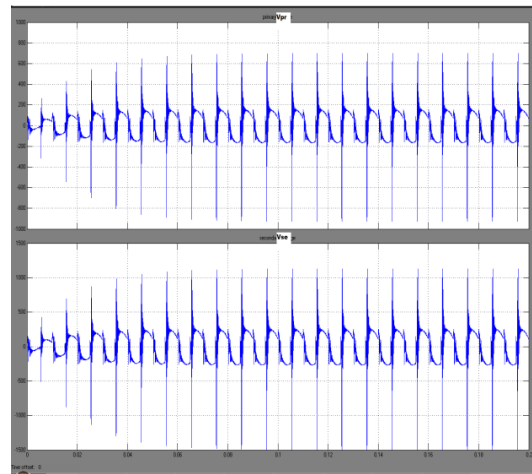
SIMULATION CIRCUIT



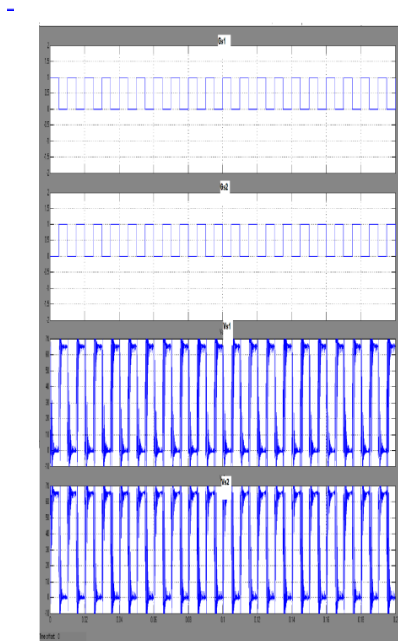
INPUT VOLTAGE



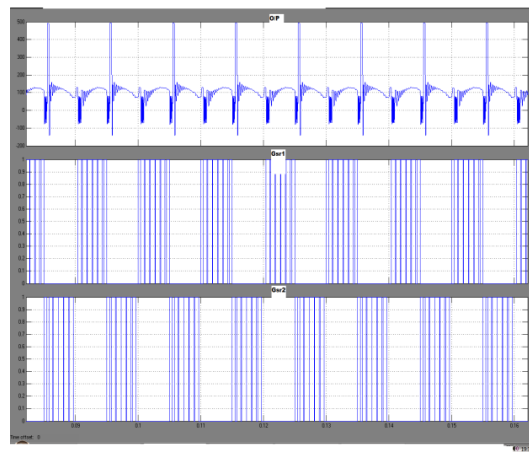
**GATING SIGNAL AND VOLTAGE
ACROSS SWITCHES**



OUTPUT WAVEFORMS



TRANSFORMER VOLTAGES



IV. CONCLUSION

This paper has shown an adjusted framework of the APWM deafening dc/dc converter topology. Its working rule and reliable state examination have been portrayed in inconspicuous component. It has been exhibited that the changed topology finishes ZVS over a more broad information voltage range than the first arrangement with the aide of execution twists and test results. The converter moreover keeps very close enduring capability from low-to-high information voltage. The use of synchronous rectifiers in the circuit results when all is said in done capability more conspicuous than 80% at 500 kHz trading repeat.

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